

Strongbow_PK

Schematics Document

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1SKUA

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Title

Cover Page

Size
A4

Document Number

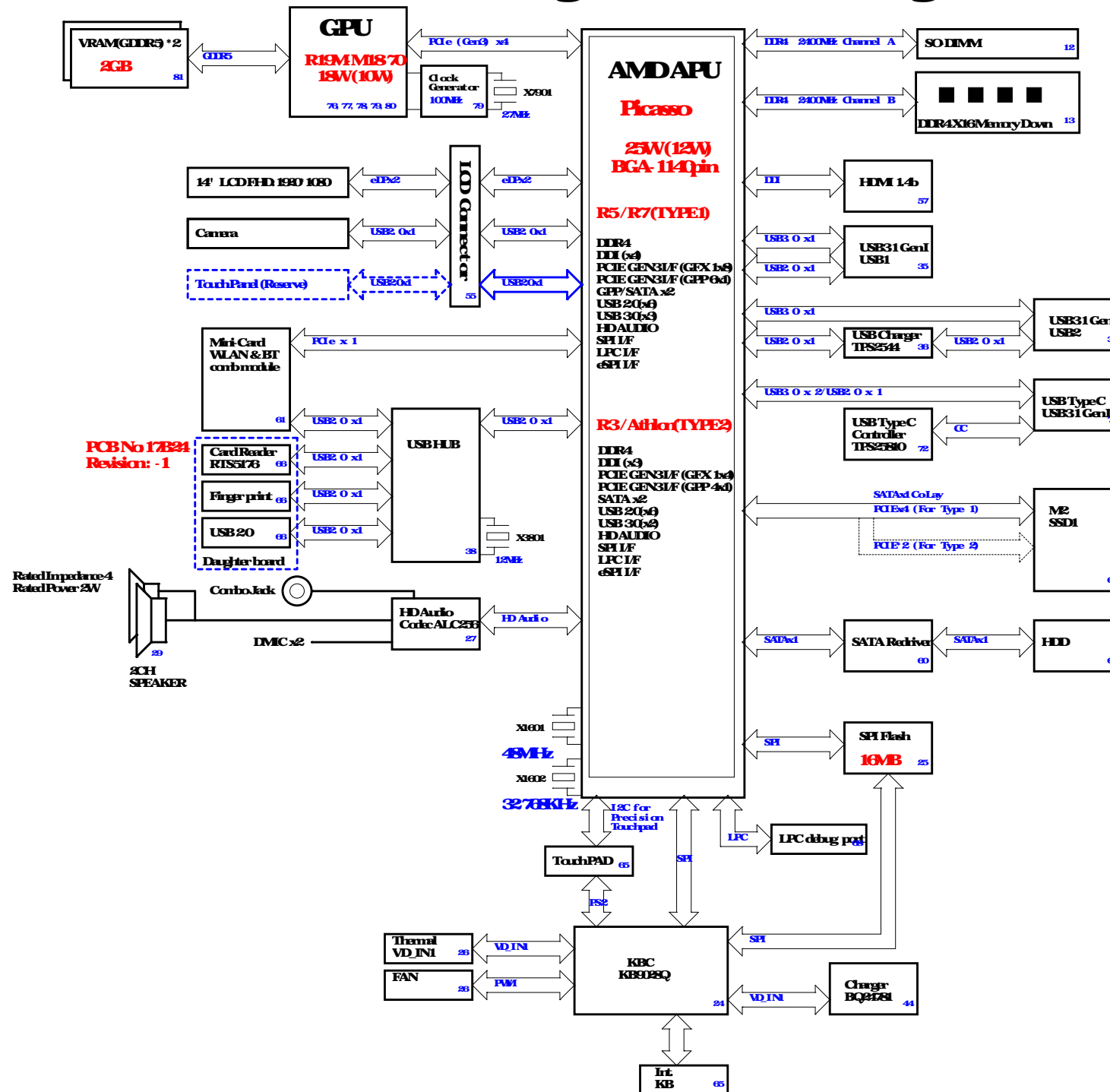
Strongbow_PK

Rev
1

Date: Wednesday, April 17, 2008

Sheet 1 of 108

Strongbow_PK Block Diagram



GPU DC/DC IS162771HRIZ 85		CHARGER BQ24781RUYR 44	
INP/UTS	OUTP/UTS	INP/UTS	OUTP/UTS
19V_D0BATOUT	VGA_CORE	19V_AD- BI+	19V_D0BATOUT
GPU DC/DC AOZ2260QI 86		SYSTEM DC/DC SY8258CRAG GP 45	
INP/UTS	OUTP/UTS	INP/UTS	OUTP/UTS
19V_D0BATOUT	1D35V_VGA_S0	19V_D0BATOUT	5V_AUX_S5 5V_S5
GPU DC/DC AOZ2260QI 86		SYSTEM DC/DC TIS513GRJER 45	
INP/UTS	OUTP/UTS	INP/UTS	OUTP/UTS
3D3V_S5	0D675V_VGA_S0	19V_D0BATOUT	3D3V_AUX_S5 3D3V_S5
GPU DC/DC RT5797A1GQW 86		GPU DC/DC IS162771HRIZ 43, 47	
INP/UTS	OUTP/UTS	INP/UTS	OUTP/UTS
3D3V_S5	1D8V_VGA_S0	19V_D0BATOUT	1V_GU_CORE
		GPU DC/DC IS162771HRIZ 43, 48	
		INP/UTS	OUTP/UTS
		19V_D0BATOUT	1D8V_GU_S0
		GPU DC/DC TIS514GRJER 51	
		INP/UTS	OUTP/UTS
		19V_D0BATOUT	1D8V_S3 2D3V_S3 0D6V_VREF_S0
		SYSTEM DC/DC AOZ2260QI 52	
		INP/UTS	OUTP/UTS
		19V_D0BATOUT	0D6V_S5
		SYSTEM Load switch G5027RDID 40	
		INP/UTS	OUTP/UTS
		1D8V_S5 1V_VCS1G	1V_VCS1G 1V_VCS1G
		SYSTEM Load switch TIS2297GD 40	
		INP/UTS	OUTP/UTS
		3D3V_S5 5V_S5	3D3V_S0 5V_S0
		1D8V_S5	1D8V_S0
		SYSTEM Load switch G5027RDID 40	
		INP/UTS	OUTP/UTS
		0D6V_S5	0D6V_S0

Blanking

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Title

CPU (RSVD)

Size
A4

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Sheet 4 of 106

SSID = CPU

DDR4
Channel A to SO DIMM

ADD CMD CIL 40
DATA CHECK 50
Misc. 40-60
DDR CLK 72
DQS 80

ADD and CLK on the same layer

CPUA

1 OF 13

DM DQ & DQS on the same layer

MA_A0	AE25	MA_ADD0	MA_DQ0
MA_A1	AE23	MA_ADD1	MA_DQ1
MA_A2	AE27	MA_ADD2	MA_DQ2
MA_A3	AE21	MA_ADD3	MA_DQ3
MA_A4	AC24	MA_ADD4	MA_DQ4
MA_A5	AC25	MA_ADD5	MA_DQ5
MA_A6	AE24	MA_ADD6	MA_DQ6
MA_A7	AC27	MA_ADD7	MA_DQ7
MA_A8	AE22	MA_ADD8	MA_DQ8
MA_A9	AC21	MA_ADD9	MA_DQ9
MA_A10	AE24	MA_ADD10	MA_DQ10
MA_A11	AA24	MA_ADD11	MA_DQ11
MA_A12	AC23	MA_ADD12	MA_DQ12
MA_A13	AE25	MA_ADD13, BANK2	MA_DQ13
MA_A14	AC27	MA_ADD14	MA_DQ14
MA_A15	AC23	MA_ADD15	MA_DQ15
MA_A16	AC23	MA_ADD16	MA_DQ16

MA_BA0	AE21	MA_BANK0	MA_DQ16
MA_BA1	AE27	MA_BANK1	MA_DQ17
MA_BG0	AA21	MA_BG0	MA_DQ18
MA_BG1	AA27	MA_BG1	MA_DQ19
MA_ACT_N	AA22	MA_ACT_L	MA_DQ20

MA_DMD	F21	MA_DMD	MA_DQ21
MA_DM0	G27	MA_DM0	MA_DQ22
MA_DM1	N21	MA_DM1	MA_DQ23
MA_DM2	N23	MA_DM2	MA_DQ24
MA_DM3	N23	MA_DM3	MA_DQ25
MA_DM4	AL21	MA_DM4	MA_DQ26
MA_DM5	AA25	MA_DM5	MA_DQ27
MA_DM6	AE21	MA_DM6	MA_DQ28
MA_DM7	AE27	MA_DM7	MA_DQ29

DM DQ & DQS on the same layer

MA_DQS_DQ0	F22	MA_DQS_DQ0
MA_DQS_DQ1	G22	MA_DQS_DQ1
MA_DQS_DQ2	H27	MA_DQS_DQ2
MA_DQS_DQ3	H23	MA_DQS_DQ3
MA_DQS_DQ4	N27	MA_DQS_DQ4
MA_DQS_DQ5	N23	MA_DQS_DQ5
MA_DQS_DQ6	P21	MA_DQS_DQ6
MA_DQS_DQ7	R21	MA_DQS_DQ7
MA_DQS_DQ8	AV26	MA_DQS_DQ8
MA_DQS_DQ9	AV27	MA_DQS_DQ9
MA_DQS_DQ10	AN24	MA_DQS_DQ10
MA_DQS_DQ11	AN25	MA_DQS_DQ11
MA_DQS_DQ12	AL23	MA_DQS_DQ12
MA_DQS_DQ13	A123	MA_DQS_DQ13
MA_DQS_DQ14	AV20	MA_DQS_DQ14
MA_DQS_DQ15	AV20	MA_DQS_DQ15

SSID = CPU

DDR4
Channel B to Memory Down

ADD CMD CIL 40
DATA CHCK 50
Misc. 40-60
DDR CLK 72
DQS 80

ADD and CLK on the samlayer

MB A0	AC30	MB ADD0
MB A1	AC32	MB ADD1
MB A2	AC30	MB ADD2
MB A3	AB29	MB ADD3
MB A4	AB31	MB ADD4
MB A5	AA30	MB ADD5
MB A6	AA29	MB ADD6
MB A7	Y30	MB ADD7
MB A8	AA31	MB ADD8
MB A9	VA29	MB ADD9
MB A10	AB29	MB ADD10
MB A11	Y32	MB ADD11
MB A12	VA31	MB ADD12
MB A13	AK30	MB ADD13, BANK2
MB WE#	AK30	MB WE_L, ADD14
MB CAS#	AK32	MB CAS_L, ADD15
MB RAS#	AK30	MB RAS_L, ADD16

MB B0	AFB1	MB BANK0
MB B1	AG32	MB BANK1
MB B20	V31	MB B20
MB B21	V29	MB B21

MB ACT_N	V30	MB ACT_L
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MB D0	C21	MB D0
MB D1	C25	MB D1
MB D2	E32	MB D2
MB D3	K30	MB D3
MB D4	AP30	MB D4
MB D5	AW31	MB D5
MB D6	BB31	MB D6
MB D7	BB22	MB D7
MB D8	N32	MB D8

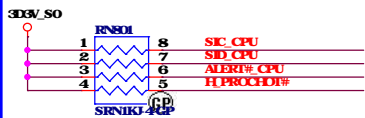
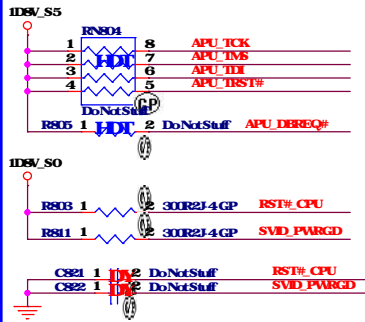
DM DQ & DQS on the same layer

MB DQ0	D22	MB DQ0
MB DQ1	B25	MB DQ1
MB DQ2	D25	MB DQ2
MB DQ3	B25	MB DQ3
MB DQ4	F29	MB DQ4
MB DQ5	F30	MB DQ5
MB DQ6	K31	MB DQ6
MB DQ7	K29	MB DQ7
MB DQ8	AK31	MB DQ8
MB DQ9	AK31	MB DQ9
MB DQ10	AA30	MB DQ10
MB DQ11	BC25	MB DQ11
MB DQ12	BA25	MB DQ12
MB DQ13	BC22	MB DQ13
MB DQ14	BA22	MB DQ14
MB DQ15	N31	MB DQ15
MB DQ16	N32	MB DQ16
MB DQ17	N32	MB DQ17
MB DQ18	N32	MB DQ18
MB DQ19	N32	MB DQ19
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MB D		

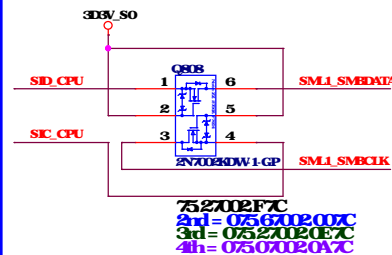
SSID = PCH

DisplayPort	Device
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1	HDMI

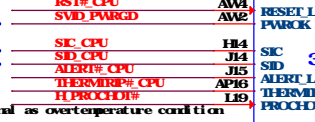
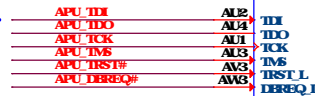
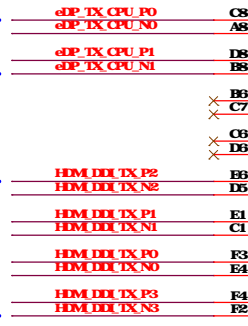
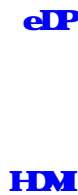
HDI PIN Pull High Resistor
ASMI If HDI CON is needs of use



SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



752702F7C
2d = 0527020E7C
3d = 0527020E7C
4d = 0527020E7C



3 OF 13

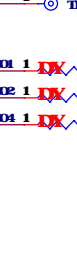
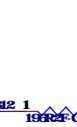
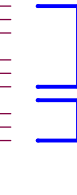
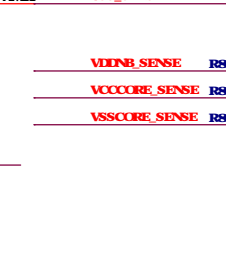
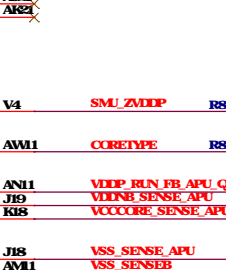
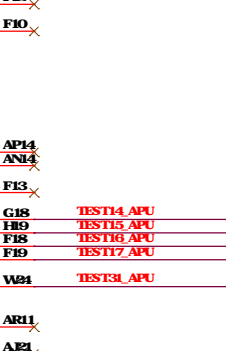
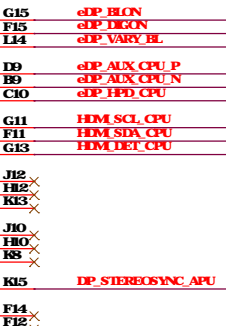
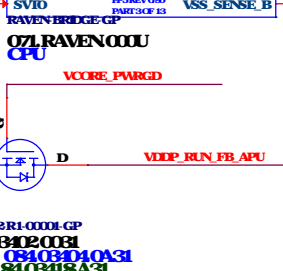
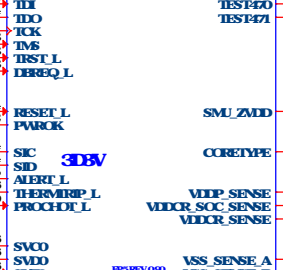
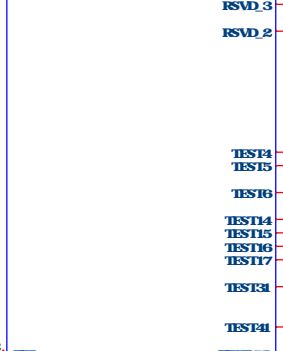
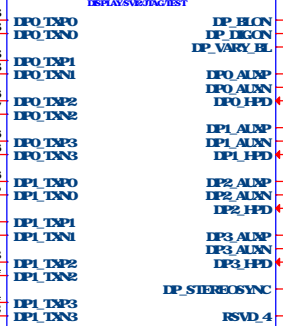
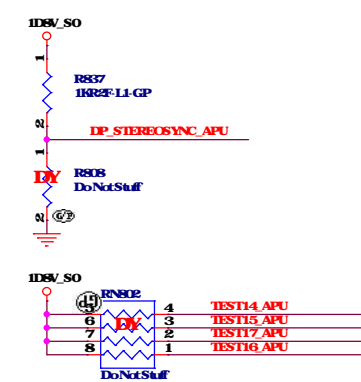


Table 4. LCD Power Interface Pin Descriptions

Signal Name	Type	Description	Pin
DP_BCON	IO	Display Panel Backlight Enable	1
DP_DCON	IO	Display Panel Power Enable	2
DP_STEREO_SYNC	IO	Signal used to drive stereo display (for 3D)	3
DP_VARY_BL	IO	Display Backlight (Variable Control)	4

Pinout	Description
DP_BCON	BL_ENABLE
DP_DCON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM

HMI: High = Enable



CPURAVEN000U

Q805
RA3402R1-00001-GP
081034020001
2d = 0810340A31
3d = 8410340A31

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Model: **Strongbow PK**

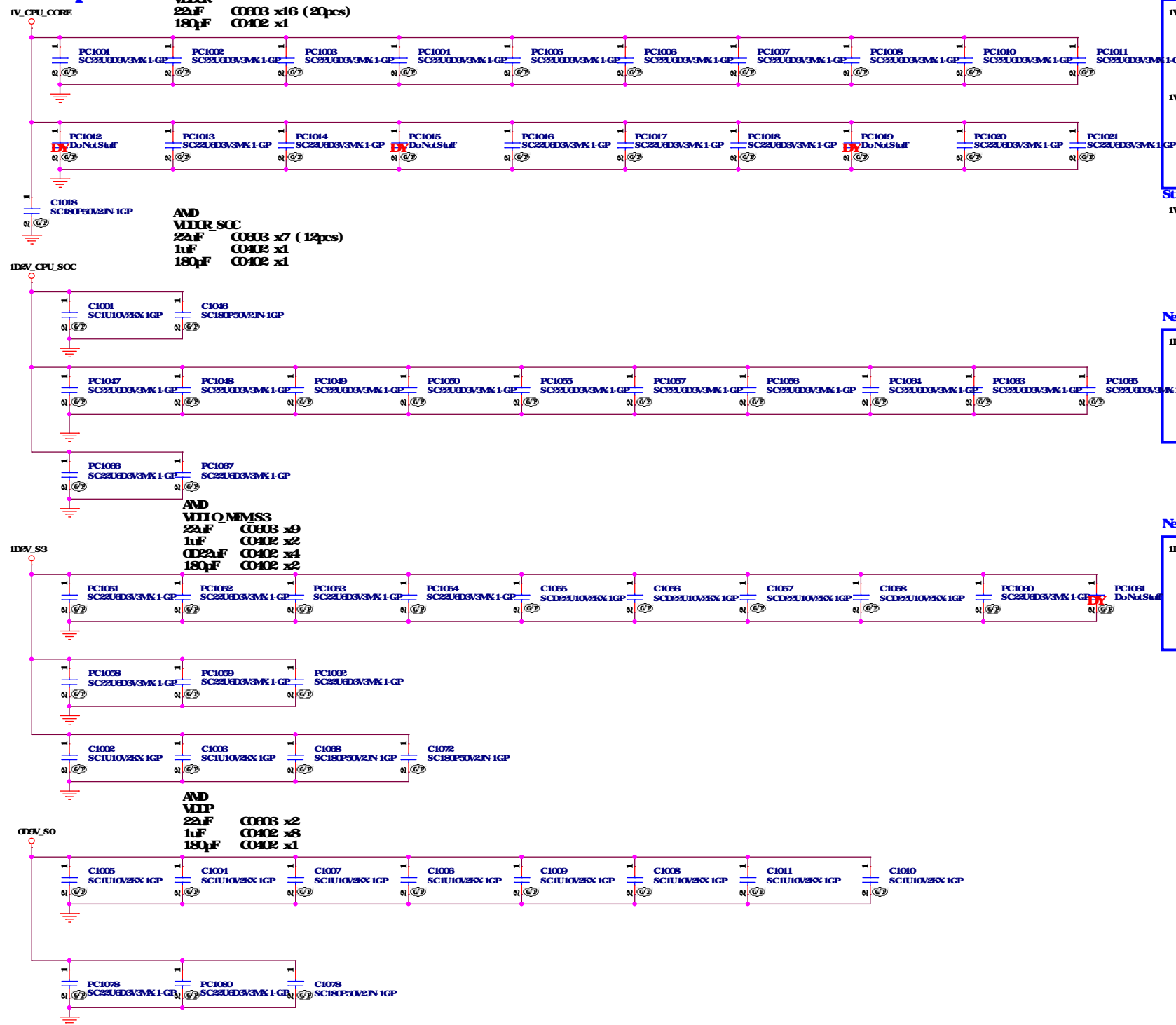
Revision: **1**

Weekend: April 17, 2013

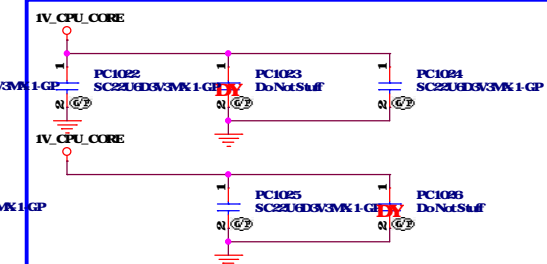


Title			
CPU (VSS)			
Site	Document Number	Rev	
A3	Strongbow_PK	1	
Date	Wednesday, April 17, 2003		Page 9 of 108

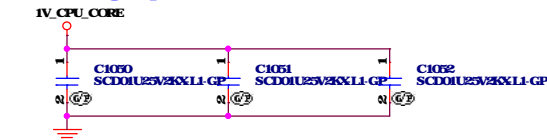
APU Caps



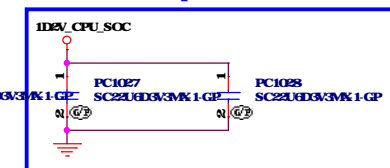
Need confirm(5pcs)



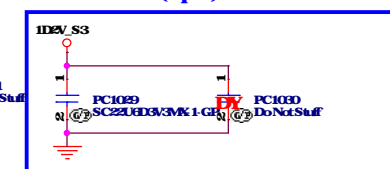
Stitching Caps



Need confirm(2pcs)



Need confirm(2pcs)



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THIS

CPU (POWER CAP1)

Size

Document Number

Strongbow_PK

Rev

Date: Wednesday, April 17, 2019

Sheet 10 of

106

APU Caps

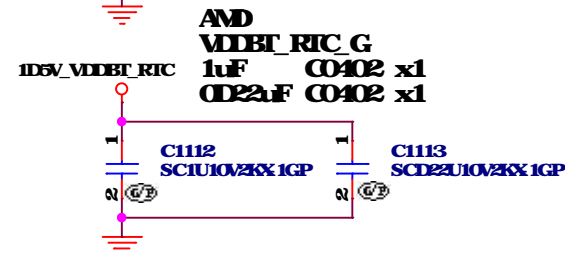
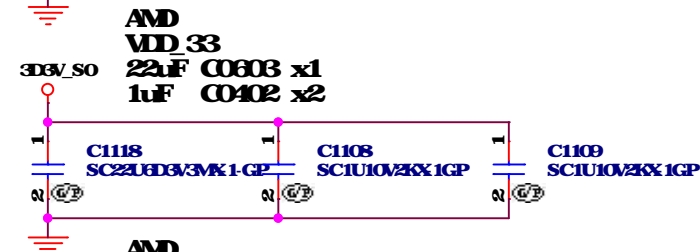
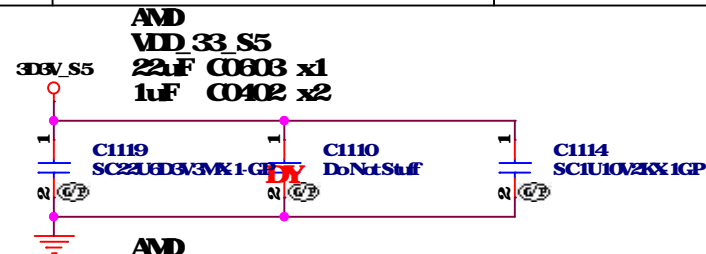
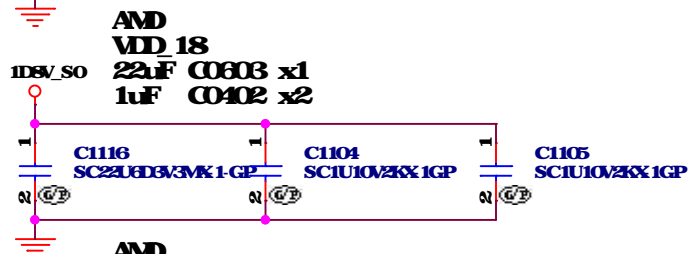
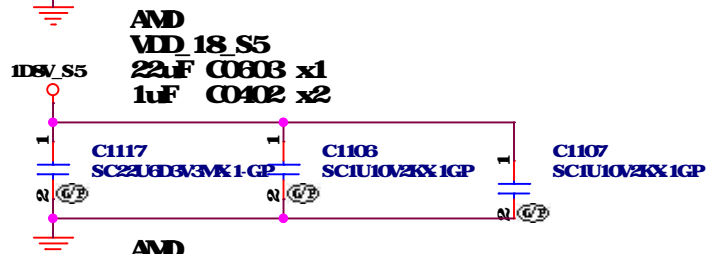
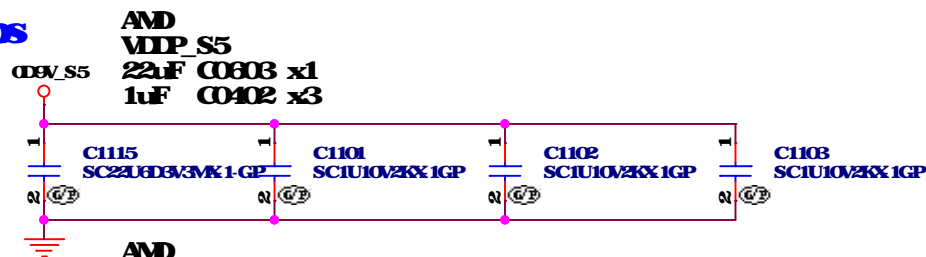


Table 110. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_S0C	VDDIO_MEM_S31,2	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 μF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 μF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 μF	0402 X5R	-	-	4(split)	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2(split)	1BU	-	-	-	-	-	-	-

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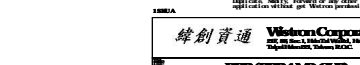
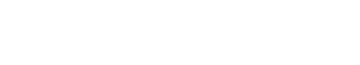
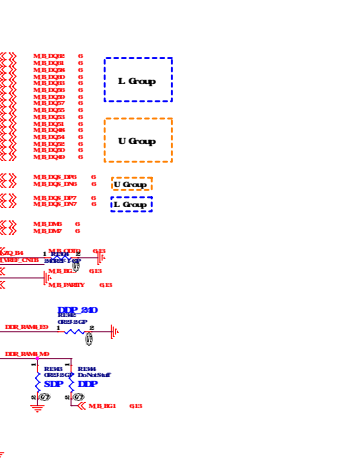
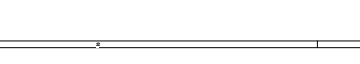
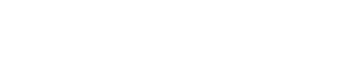
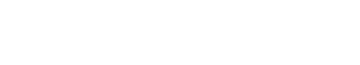
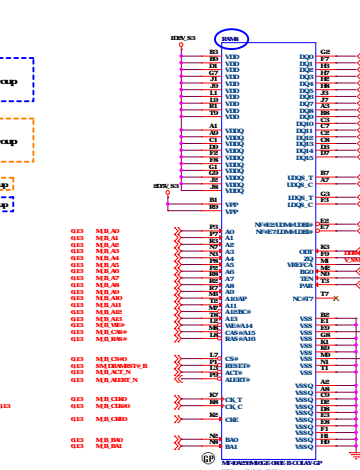
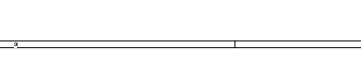
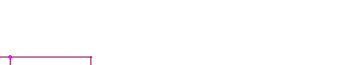
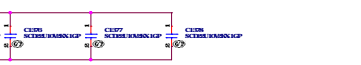
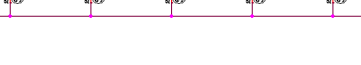
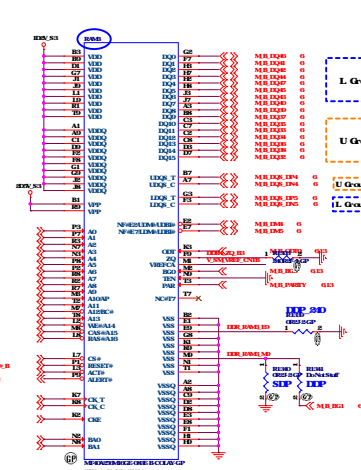
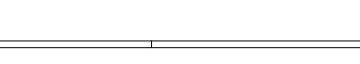
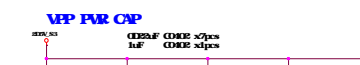
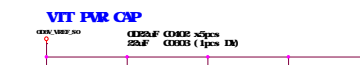
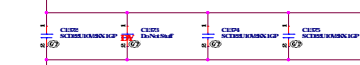
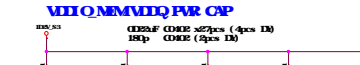
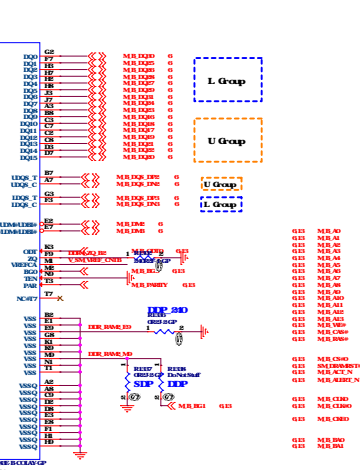
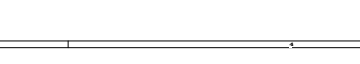
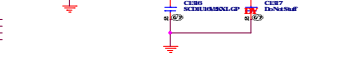
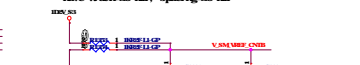
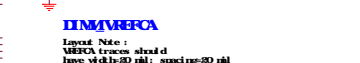
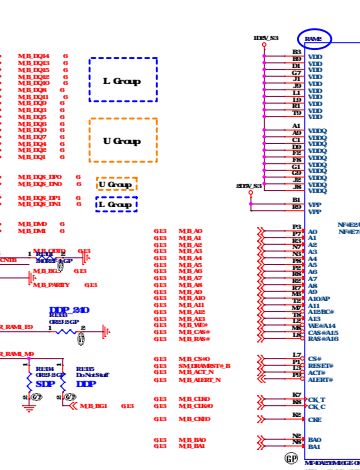
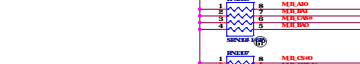
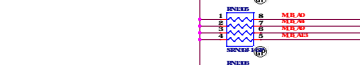
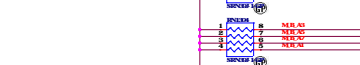
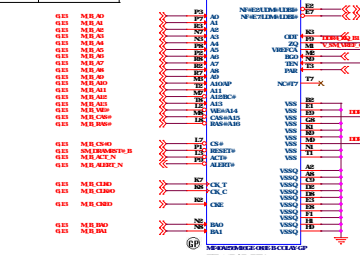
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Title CPU (POWER CAP2)			
Size A4	Document Number Strongbow_PK		Rev 1
Date Wednesday, April 17, 2019		Sheet 11	of 106

Wednesday, April 17, 2019 Sheet 12 of 106

Main Func = DDR4

DQ0	DQ-DQ7
DQ8	DQ8-DQ15
DQ16	DQ16-DQ23
DQ24	DQ24-DQ31
DQ32	DQ32-DQ39
DQ40	DQ40-DQ47
DQ48	DQ48-DQ55
DQ56	DQ56-DQ63



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Size
A4

Document Number

Strongbow_PK

Rev
1

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Title

DDR (RSVD)

Size
A4

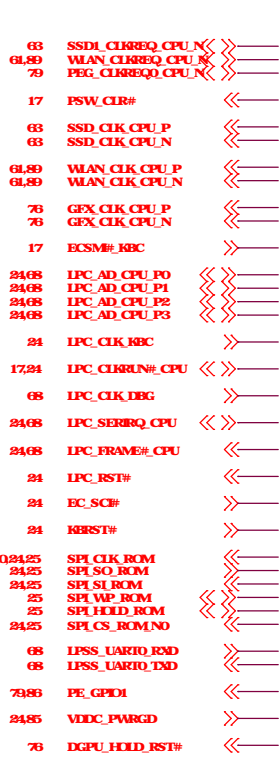
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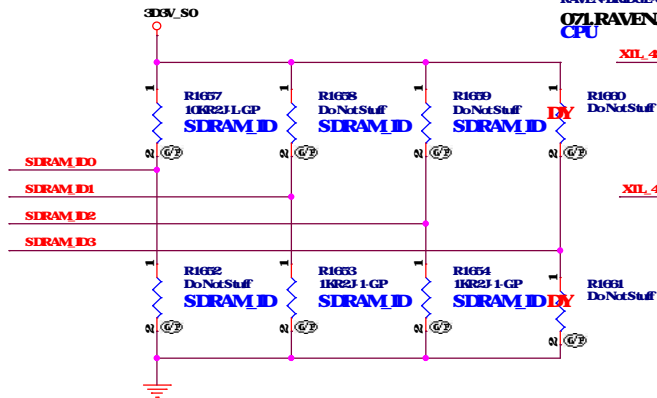
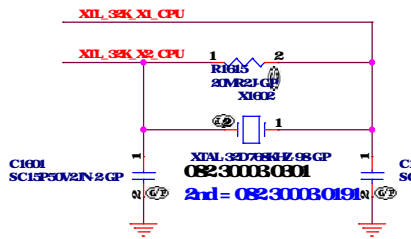
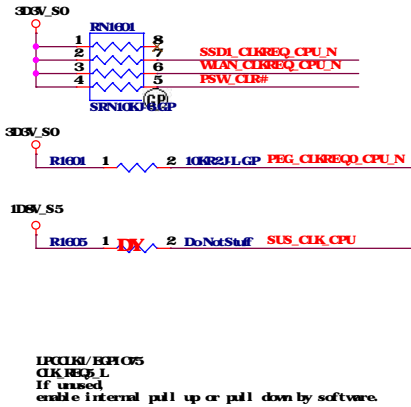
Rev
1

Date: Wednesday, April 17, 2009

Sheet 15 of 108



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15	16	17	18	19
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380V/50V

1A

R177
D3805A1F
UMA

0.1F

DGRU155N1F

250V/0.1A

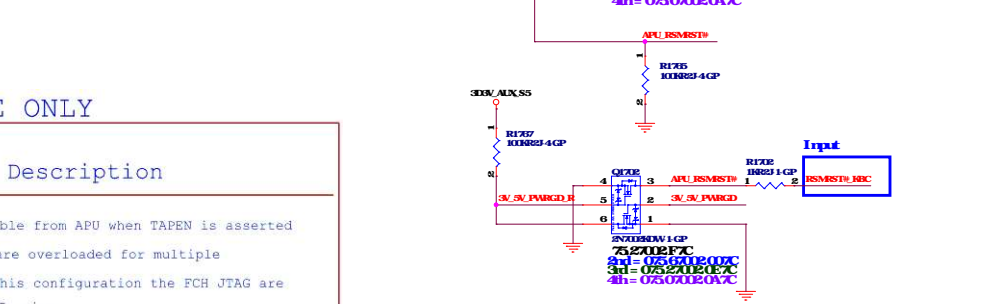
1A

R175
H0R251GP
PX

0.1F

+5V

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



Traps	LRRAME.L LPCCLDRDGE0P91 LPCCLDRGEP075 RTECLK SYS_RESET_LAGW0H RUNKUBR_CZT_LAGP0H ACPI03
SOPWR Bail	AGPIO0 - EGPIO8
SOPWR Bail	AGPIO0H - EGPIO8-05
SMBQ_300H_S0	TRM4
SMB1_300H_S5	RBC_300H_S5 Thermal_300H_S0 SENSOR for HDD Protect
APU Type 1only	AGPIE0AGPIO0
APU type 2Only	

TYPE C

Main Func = USB

73 USB3_USB30_TX_P0
73 USB3_USB30_TX_N0
73 USB3_USB30_RX_P0
73 USB3_USB30_RX_N0

73 USB3_USB30_RX_P1
73 USB3_USB30_RX_N1
73 USB3_USB30_TX_P1
73 USB3_USB30_TX_N1

TYPE C USB20

73 USB3_USB30_P
73 USB3_USB30_N

USB3_0 Port 1

35 USB1_USB30_TX_P
35 USB1_USB30_TX_N
35 USB1_USB30_RX_P
35 USB1_USB30_RX_N

35 USB1_USB30_P
35 USB1_USB30_N

USB3_0 Port 2

35 USB2_USB30_TX_P
35 USB2_USB30_TX_N
35 USB2_USB30_RX_P
35 USB2_USB30_RX_N

35 USB2_USB30_P
35 USB2_USB30_N

CCD

55 CCD_USB30_P
55 CCD_USB30_N

USB 2_0

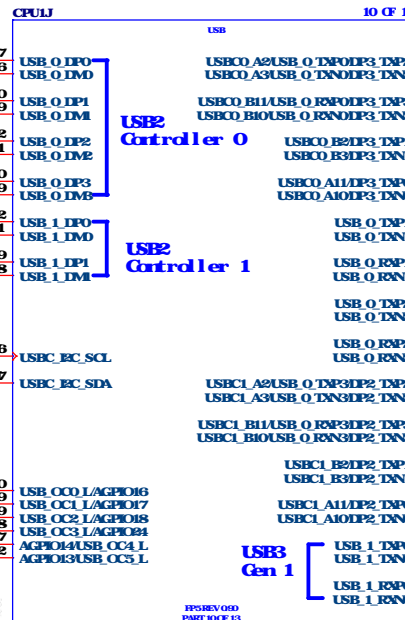
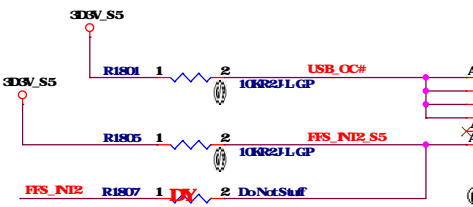
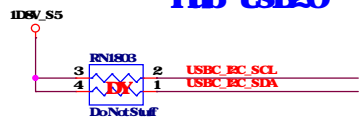
6689 USB4_USB30_P
6689 USB4_USB30_N

Hb USB20

38 HUB_USB30_P
38 HUB_USB30_N

17 FFS_IND2

Type C
USB3_0 Port 1
USB3_0 Port 2
CCD
USB 2_0
Hb USB20



RAVENBRIDGE GP
07L RAVEN000U
CPU

AGPI013/USB CC5_L

If unused, enable internal pull up or pull down by software.

Type C
USB3_0 Port 1
USB3_0 Port 2

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CPU (USB)		
Rev: AC3	Revision Number: Strongbow PK	Rev: 1
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CPU (RSVD)

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Document Number

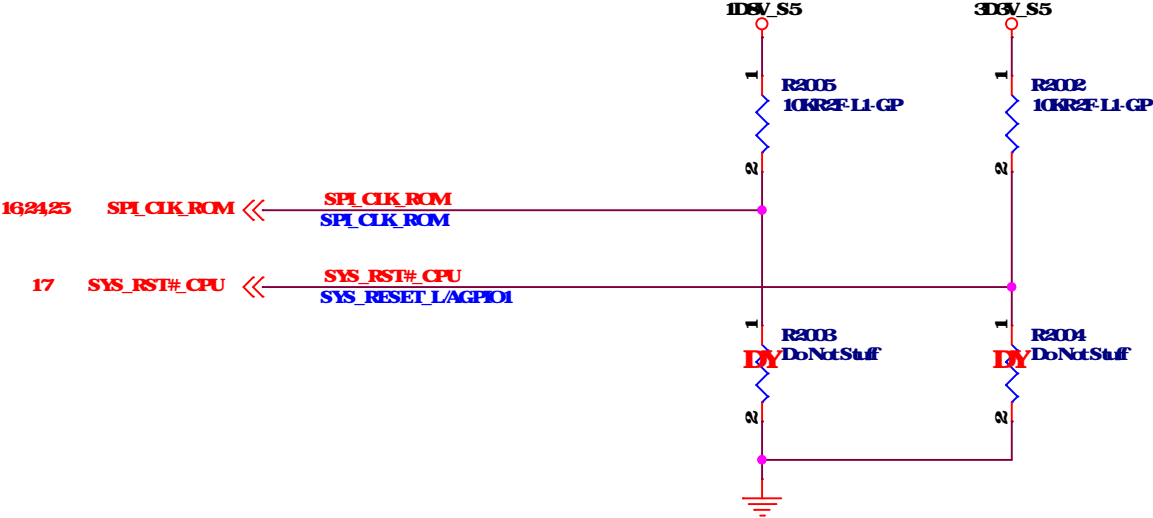
Strongbow_PK

Rev
1

Date: Wednesday, April 17, 2009

Sheet 19 of 108

STRAP PINS



	PN SPI_CLK NETSPI_CLK_ROM	PNSYS_RESET_L//AGPIO1 NETSYS_RST#_CPU
PULL Up	Configured for internal clock generator 10k (± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10K (± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL Down	Reserved	Reserved

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CPU (Strap)					
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		Strongbow_PK			1
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Size
A4

Document Number

Strongbow_PK

Rev
1

Date: Wednesday, April 17, 2009

Sheet 23 of 106

Power

- CHRG_AUX_NBC
- CHRG_AUX
- CHRG_AUX_NBC

Signal

- CHRG_AUX_NBC
- CHRG_AUX
- CHRG_AUX_NBC

GPIO High Active

- CHRG_AUX_NBC
- CHRG_AUX
- CHRG_AUX_NBC

3.3V

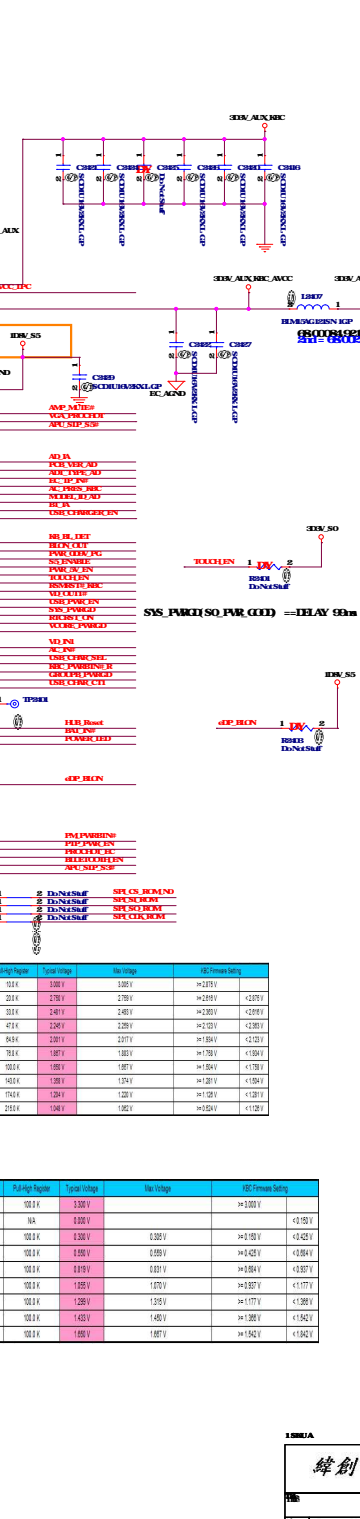
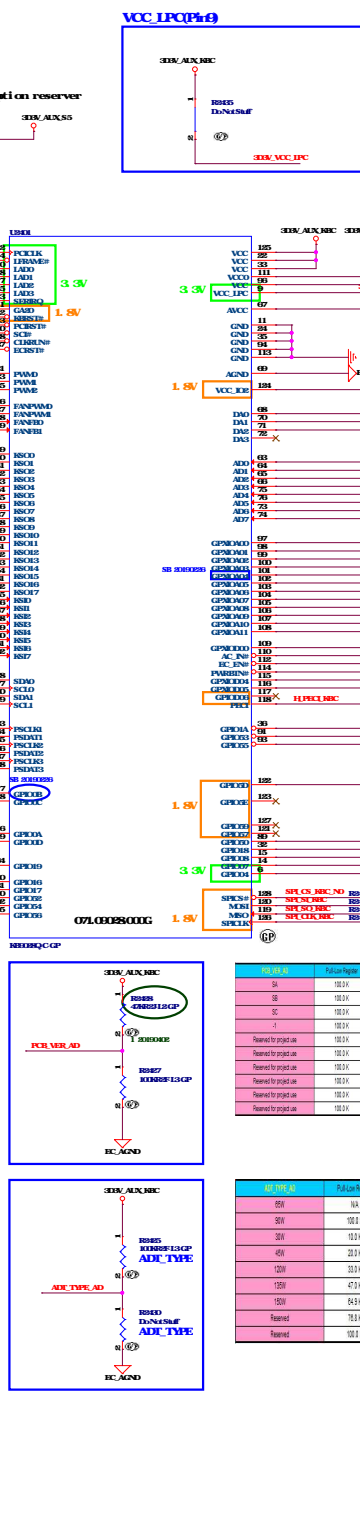
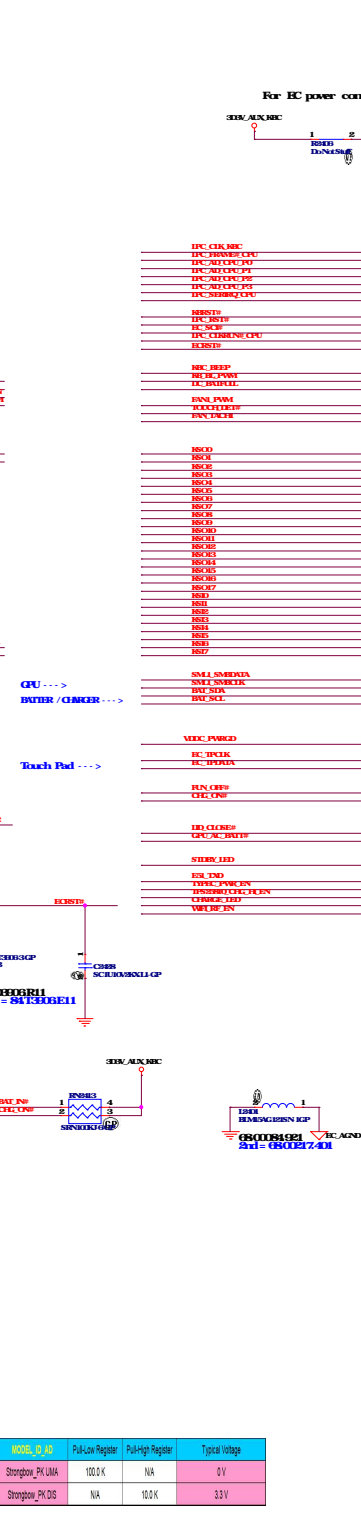
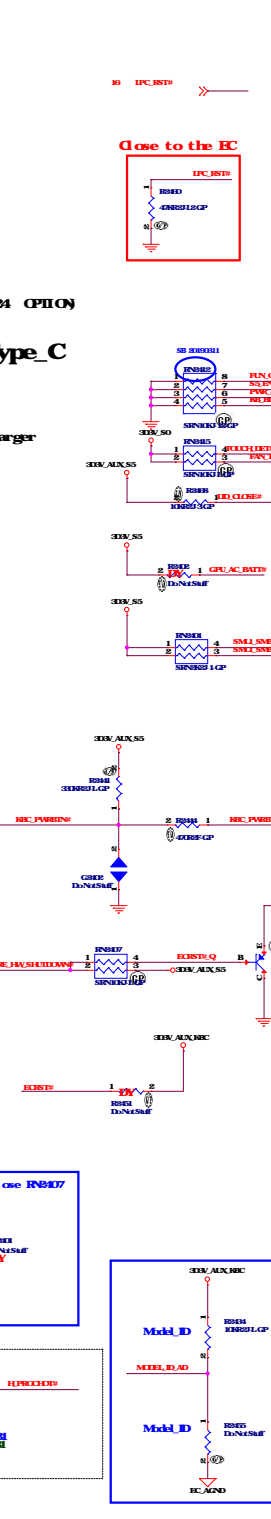
- CHRG_AUX_NBC
- CHRG_AUX
- CHRG_AUX_NBC

Type_C

- CHRG_AUX_NBC
- CHRG_AUX
- CHRG_AUX_NBC

Charger

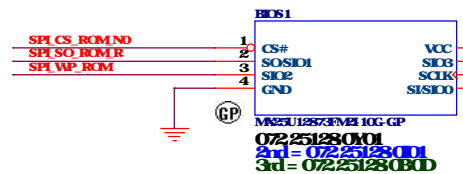
- CHRG_AUX_NBC
- CHRG_AUX
- CHRG_AUX_NBC



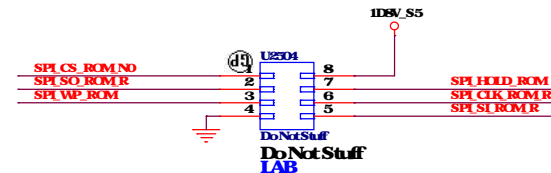
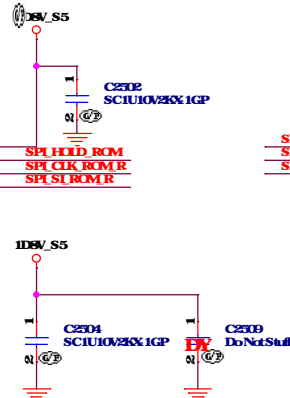
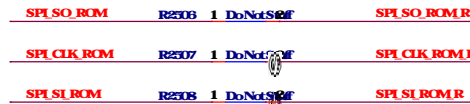
Part Number	Package	Pin Count	Typical Voltage	Max Voltage	Min Voltage
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V
SSID = KBC	100-Pin	100	1.00V	1.00V	1.00V

1624	SPI_CS_ROM0	《《	《《
1624	SPI_SO_ROM	《《	《《
16	SPI_WP_ROM	《《	《《
16	SPI_HOLD_ROM	《《	《《
1624	SPI_CLK_ROM	《《	《《
1624	SPI_SI_ROM	《《	《《
17	RTC_DET#	《《	《《
24	RTC_RST_ON	《《	《《

SPI ROMEqual length need to less than 500ml



MEC ME25UI2873FMI-10G
WINBOND VE5Q128FVSI Q
GD GD25UB128DSI GR



Width=20mil s

1 20190319

3D3V_AUX_S5

3D3V_RIC_VCC

3D3V_RIC_AUX

RIC1

GP

ACES-CO2-20 GPU

20F1639.002

2nd = 20F1841.002

R2302

1K R2302 1-L GP

3D3V_RIC_PWR

BAT54C 12 GP

7500054A7D

2nd = 07500054B7D

3rd = 0750005407D

R2304

10M R2304 1-L GP

RIC_DET

GP

Q2305

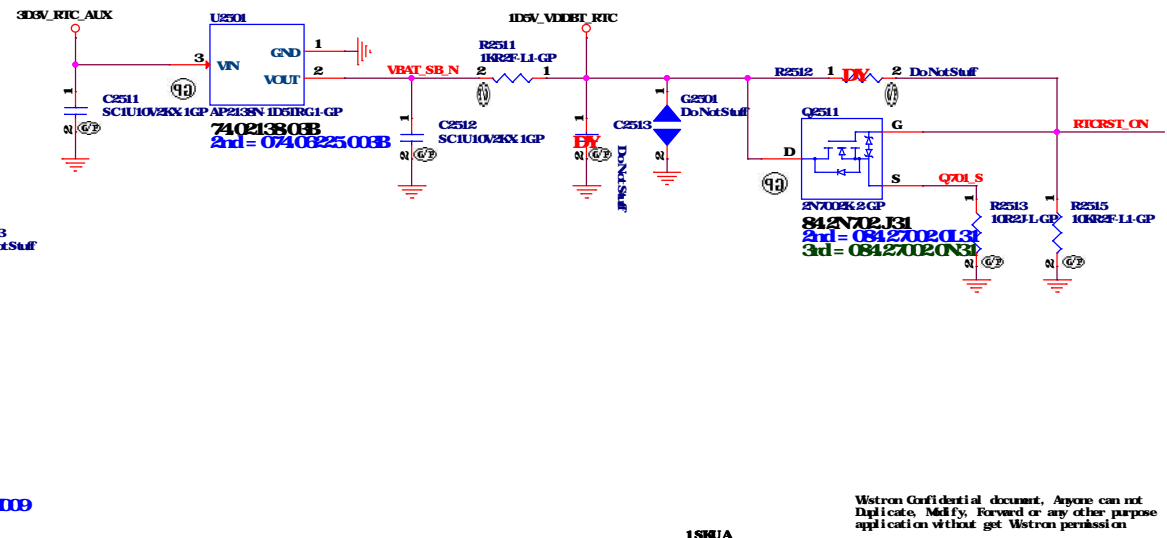
PIA2002HRI-00004-1 GP

0840702.M002

2nd = 08427002.M009

Vth(max) = 3.0V

1st= 23 21212 042
2nd= 023 22032 0611



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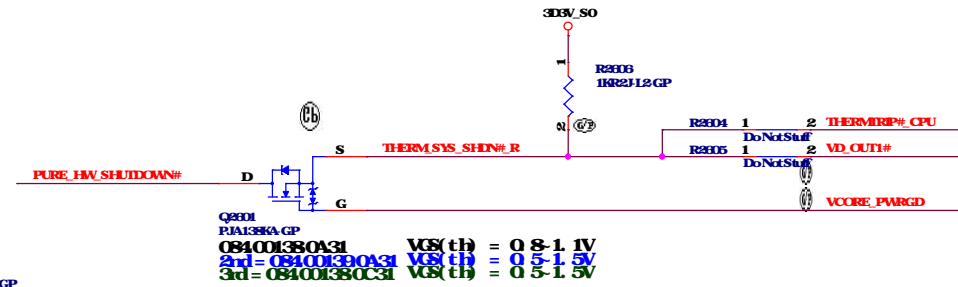
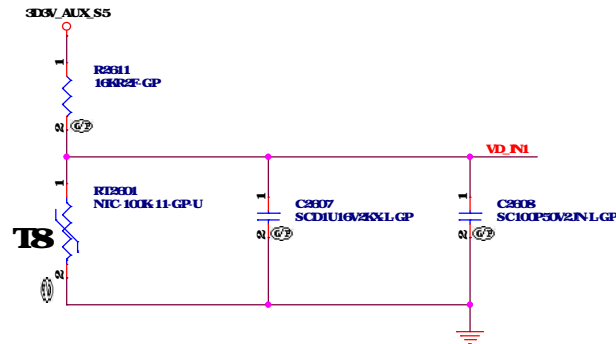
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Flash/RIC		
Site A3	Strongbow PK	Rev 1
Wednesday, April 17, 2008		2% of 100

SSID = Thermal

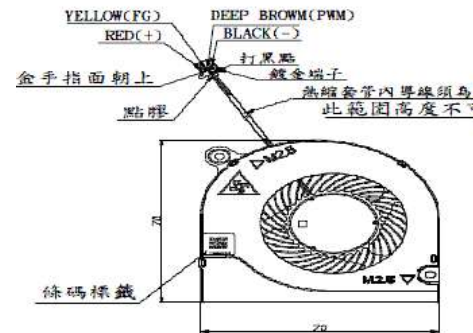
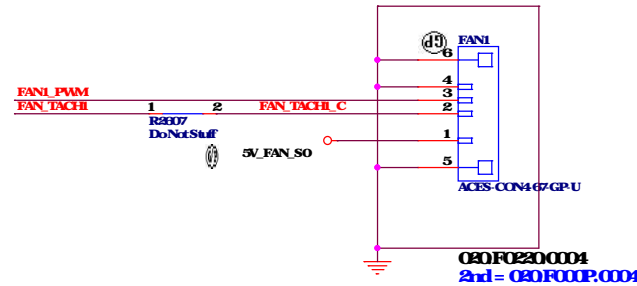
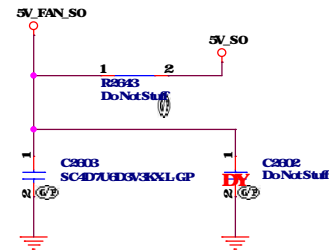
24 VD_INI
2440 PURE_HV_SHUTDOWN#
S THERMIRP#_CPU
24 VD_OUT1#
S2446 VCORE_PWROD

2489 FAN1_PWM
24 FAN_TACH1
89 FAN_TACH1_C



RI2601 close CPU and Vcore choke
VD_INI trace 10 mil

Layout: 15 mil



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700	NTIO(THERMAL/Fan)	Rev
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700	Wednesday, April 17, 2013	1 of 108

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Audio (RSVD)

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Document Number

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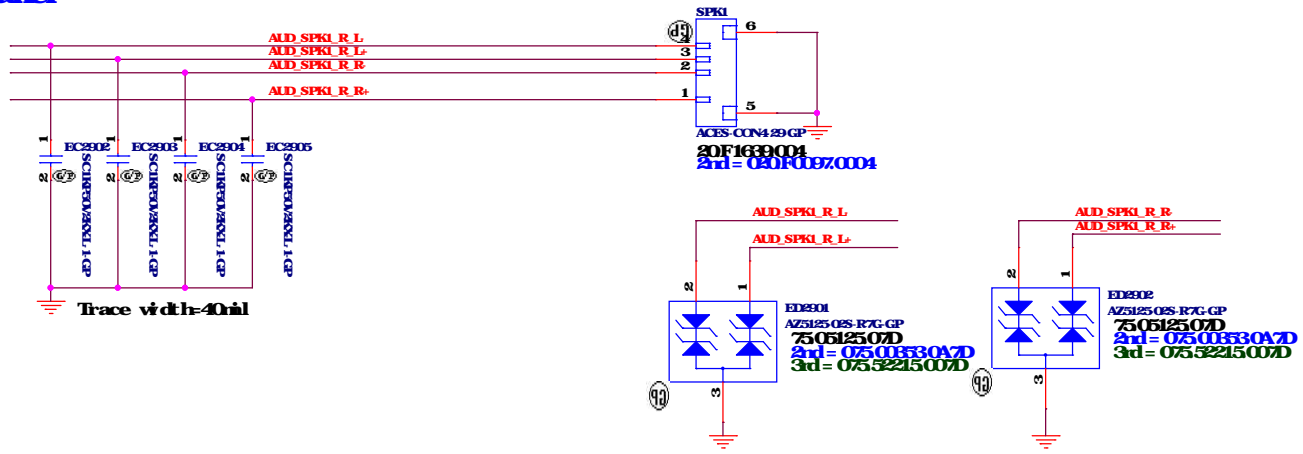
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Sheet 28 of 108

SSID = AUDIO

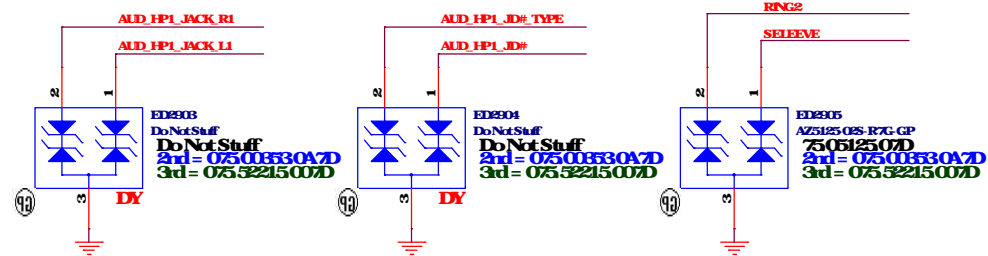
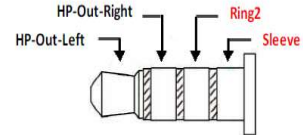
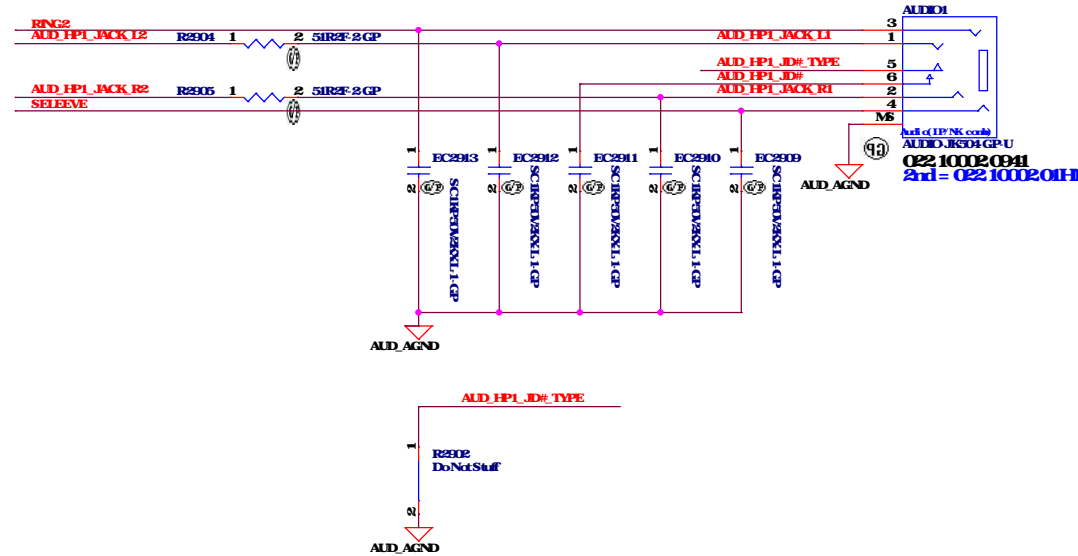
Speaker

27,80 AUD_SPK1_R_L
27,80 AUD_SPK1_R_L+
27,80 AUD_SPK1_R_R
27,80 AUD_SPK1_R_R+



27,80 RING2
27 AUD_HPL_JACK_L2
27,80 AUD_HPL_ID#
27 AUD_HPL_JACK_R2
27,80 SELEVE

80 AUD_HPL_JACK_L1
80 AUD_HPL_JACK_R1
80 AUD_HPL_ID#_TYPE



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Sheet 31 of 106

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CARDREADER (RSVD)

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Title

USB (RSVD)

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A4

Document Number

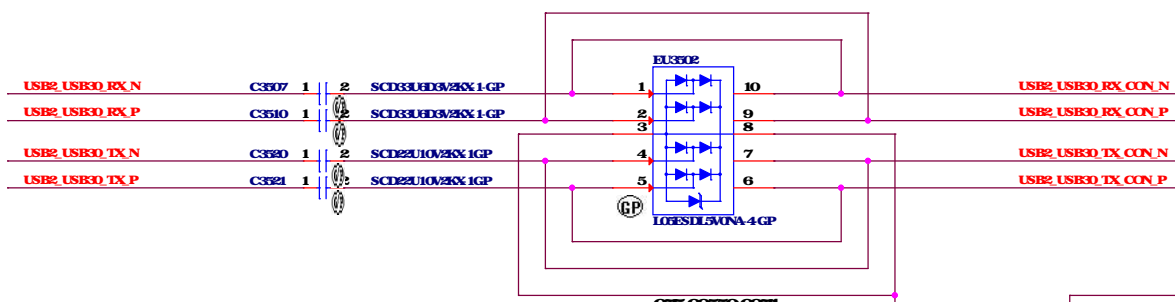
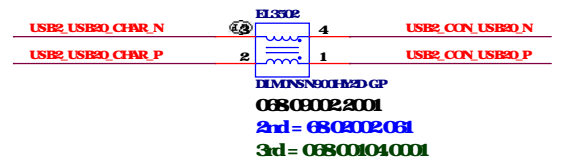
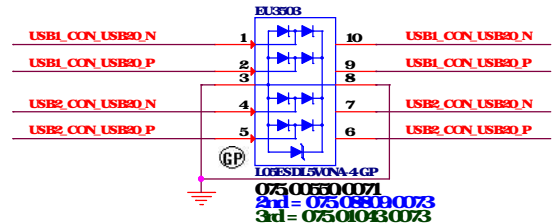
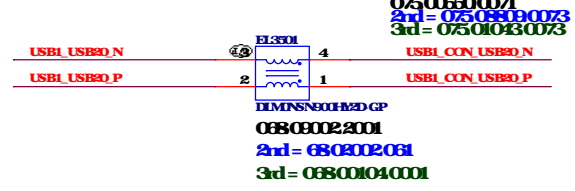
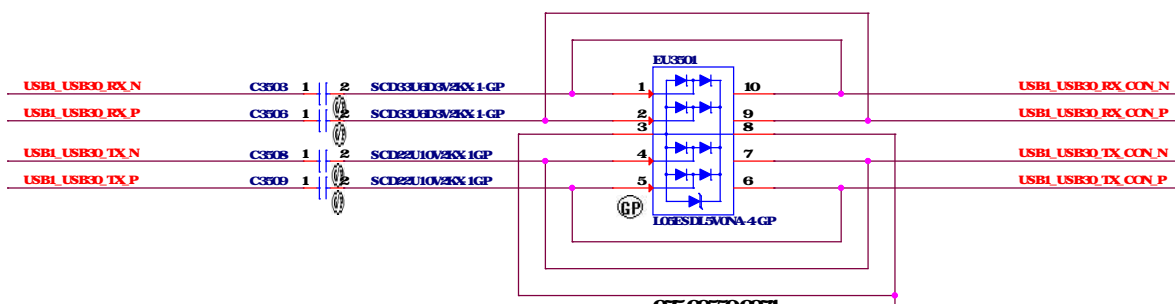
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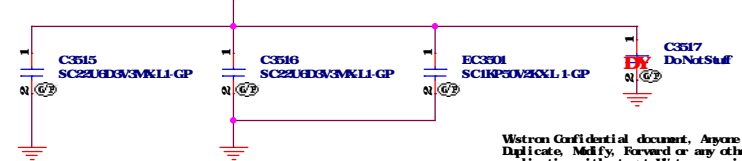
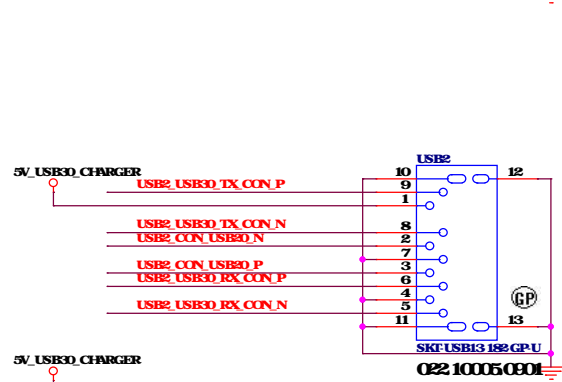
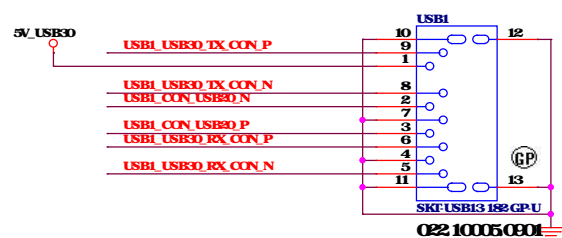
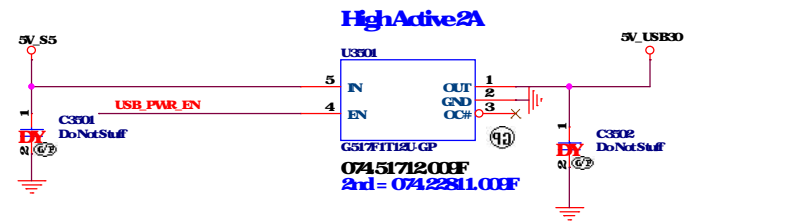
Sheet 34 of 106

24GB USB_PWR_EN >>>
 18 USB1_USB30_RX_N >>>
 18 USB1_USB30_RX_P >>>
 18 USB1_USB30_TX_N >>>
 18 USB1_USB30_TX_P >>>
 80 USB1_CON_USB30_N >>>
 80 USB1_CON_USB30_P >>>



36 USB2_USB30_CHAR_N >>>
 36 USB2_USB30_CHAR_P >>>
 18 USB2_USB30_RX_N >>>
 18 USB2_USB30_RX_P >>>
 18 USB2_USB30_TX_N >>>
 18 USB2_USB30_TX_P >>>
 80 USB2_CON_USB30_N >>>
 80 USB2_CON_USB30_P >>>

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX SuperSpeed RX
6	StdA_SSRX-
7	GND
8	StdA_SSTX SuperSpeed TX
9	StdA_SSTX-



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USB (RSVD)

Size
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Document Number

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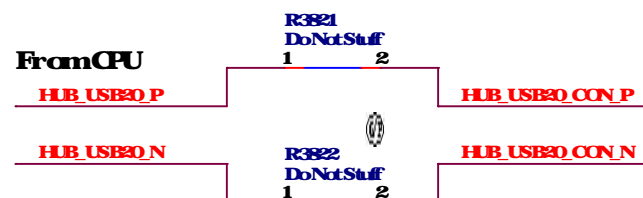
Rev
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Date: Wednesday, April 17, 2009

Sheet 37 of 106

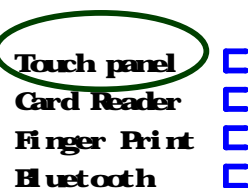
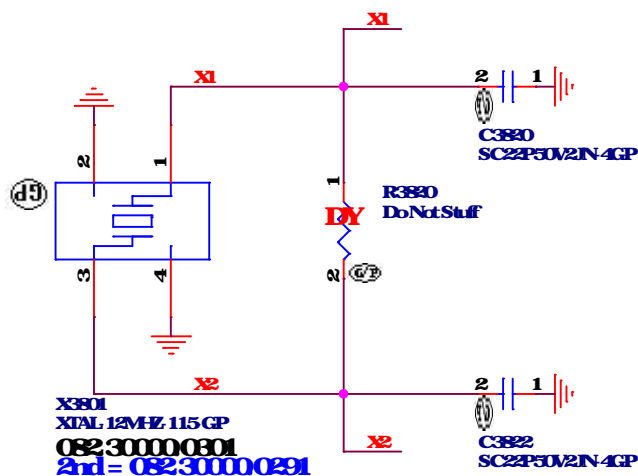
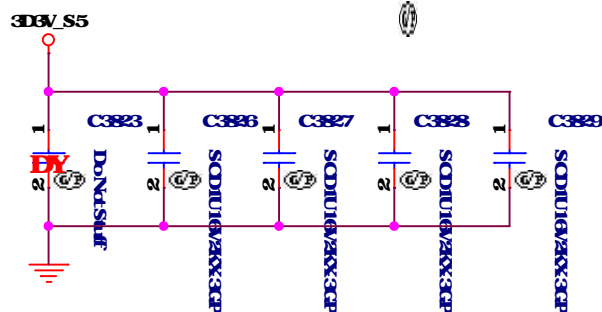
Min Func = USB HUB

18	HUB_USB20_P	⋈	---
18	HUB_USB20_N	⋈	---
55	TS_USB20_P	⋈	---
55	TS_USB20_N	⋈	---
6689	CR_USB20_P	⋈	---
6689	CR_USB20_N	⋈	---
6689	FP_USB20_P	⋈	---
6689	FP_USB20_N	⋈	---
6189	BT_USB20_P	⋈	---
6189	BT_USB20_N	⋈	---
24	HUB_Reset	⋈	---



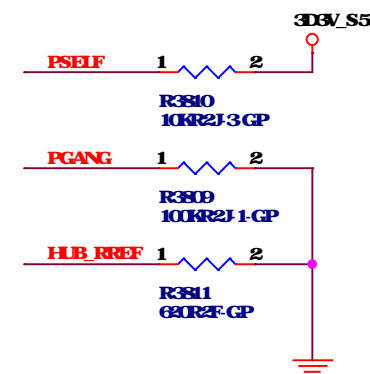
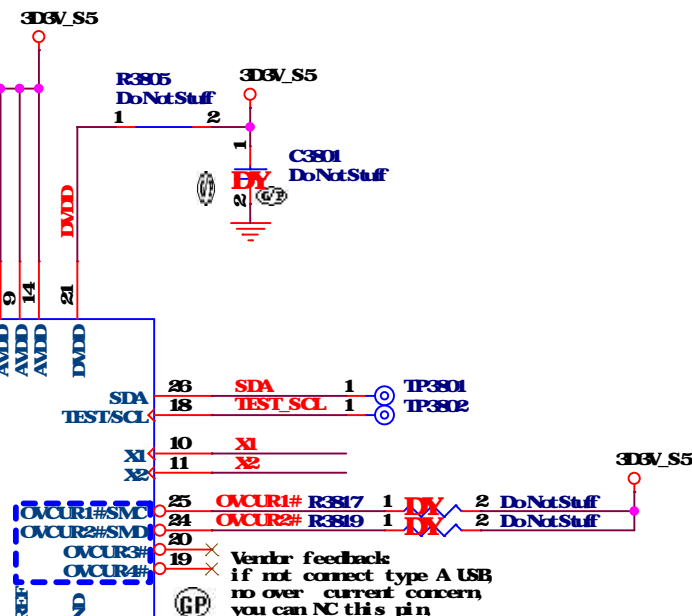
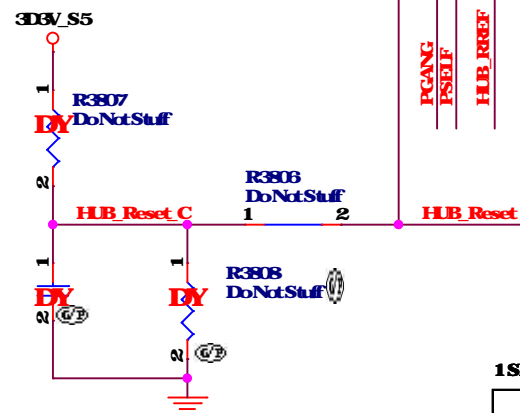
1 20190318

Touch panel
Card Reader
Finger Print
Bluetooth



HUB_USB20_CON_P	2	DP0
HUB_USB20_CON_N	1	DP1
TS_USB20_P	4	DM0
TS_USB20_N	3	DM1
CR_USB20_P	7	DM2
CR_USB20_N	6	DM3
FP_USB20_P	13	DM4
FP_USB20_N	12	DM5
BT_USB20_P	16	DM6
BT_USB20_N	15	DM7

GI850G-CH50GP
07L0850G.0008



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A4				1
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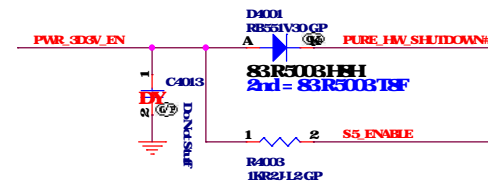
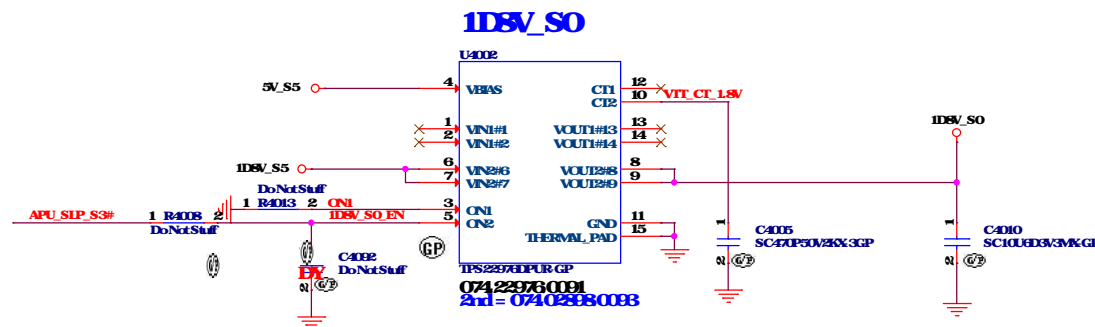
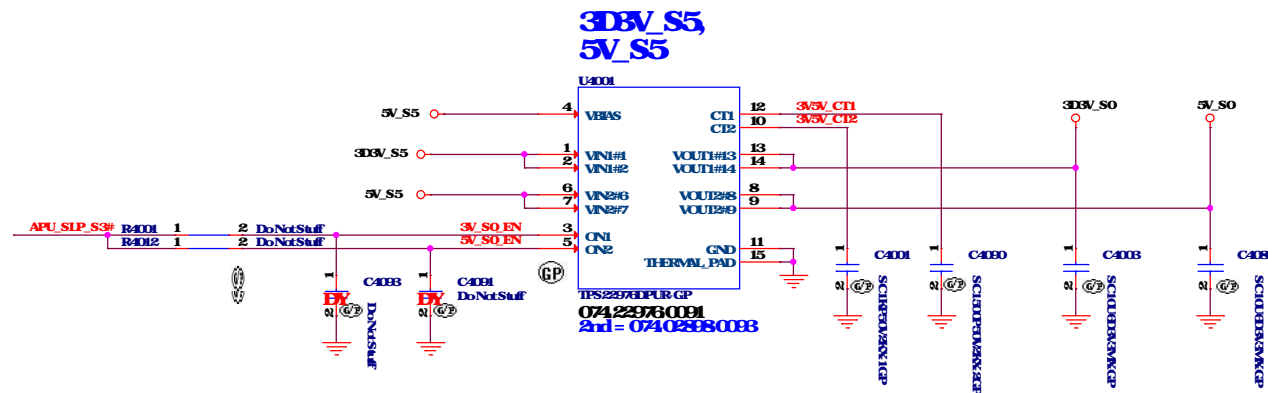
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1

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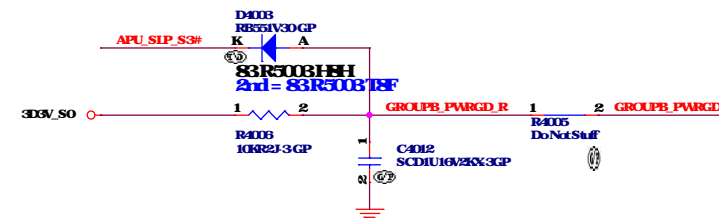
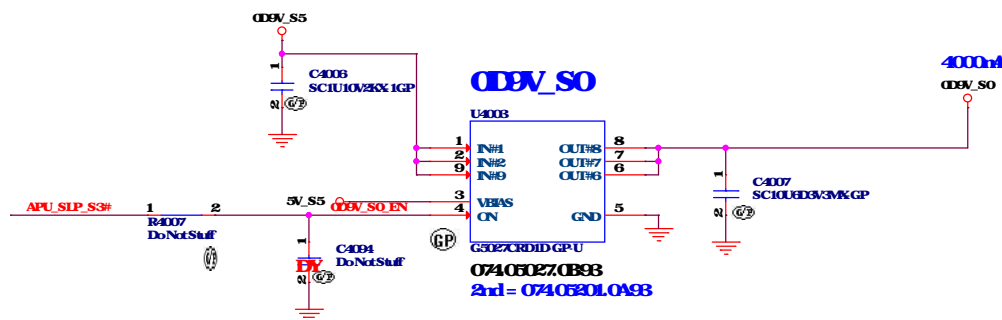
Sheet 39 of 106

Power Sequence

- 17,24,51,60 APU_SLP_S3# >>
- 45 PWR_3DV_EN >>
- 24,26 PURE_HV_SHUTDOWN# >>
- 24 S5_ENABLE >>
- 17,24 SYS_PWARGD >>
- 24,46 GROUPB_PWARGD >>



Delay for S0_PWARGD to VCORE_EN



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1580/A

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Sequence (Power Plane EN)

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Title

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Size
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Document Number

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Rev
1

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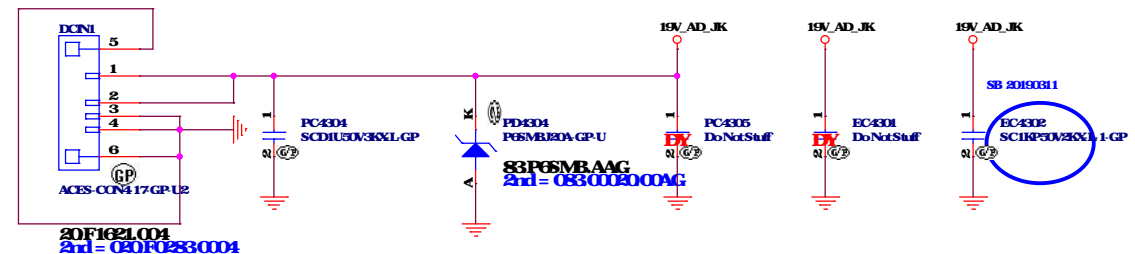
Sheet 42 of 103

2444 BAT_SCL
2444 BAT_SDA
2444 BAT_N#

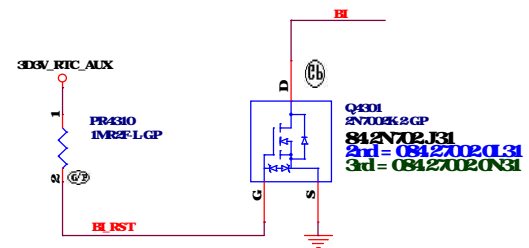
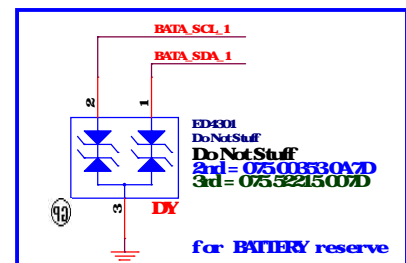
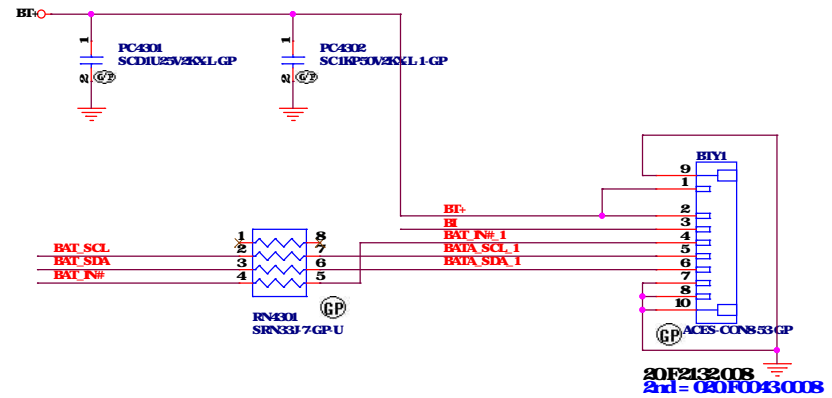
80 BL
80 BAT_N#_1
80 BATA_SCL_1
80 BATA_SDA_1
6680 BL_RST

ANNE sdution

Adaptor in to generate DOBATOUT



BATTERY CONECTOR



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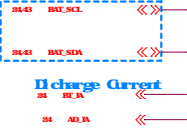
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Strongbow PK			
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OFFPAGE

SSID = Charger

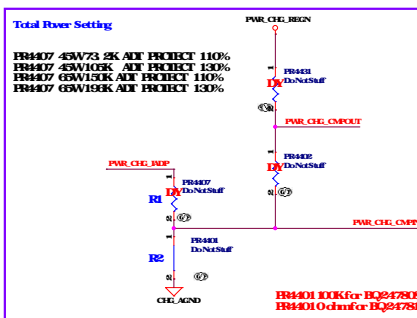
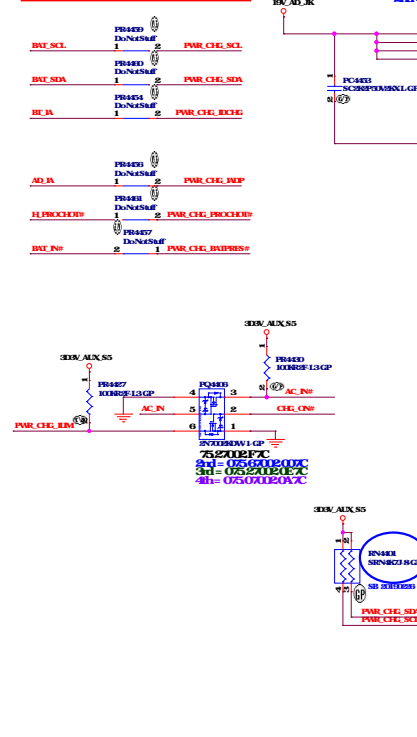
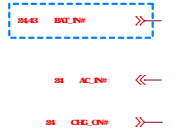
PH on EE Side



PH on EE Side

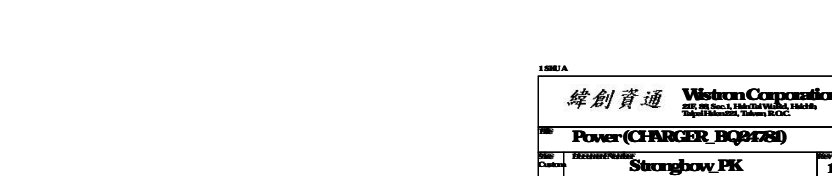
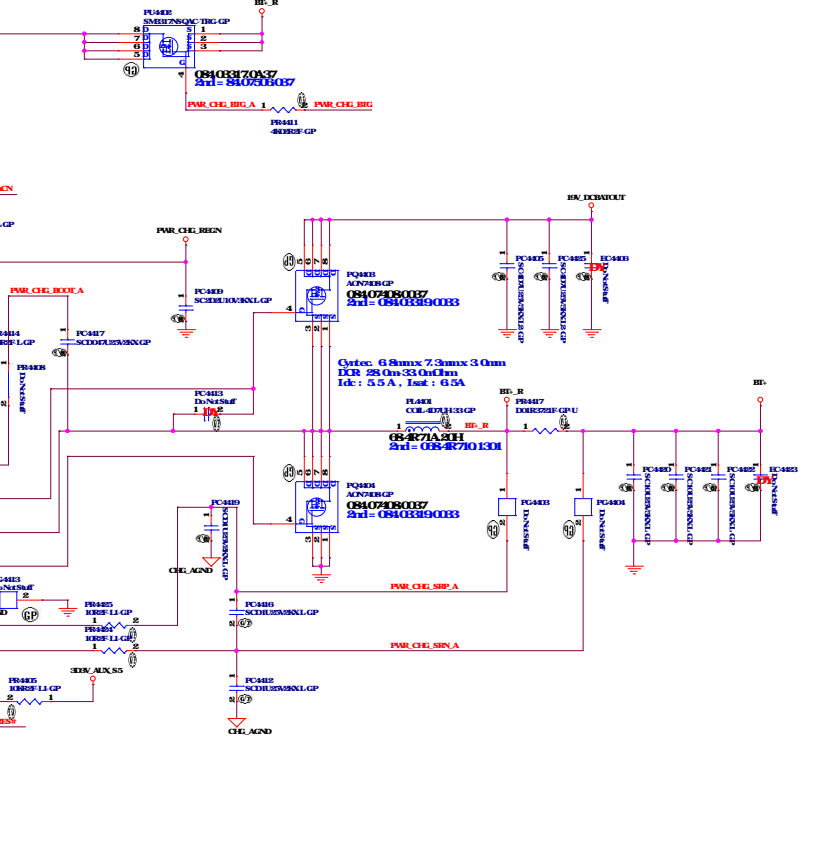
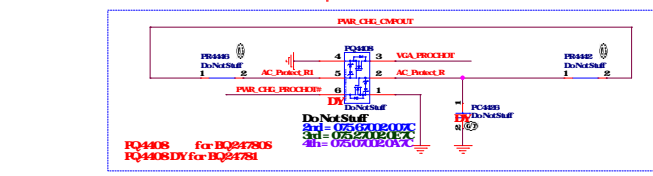


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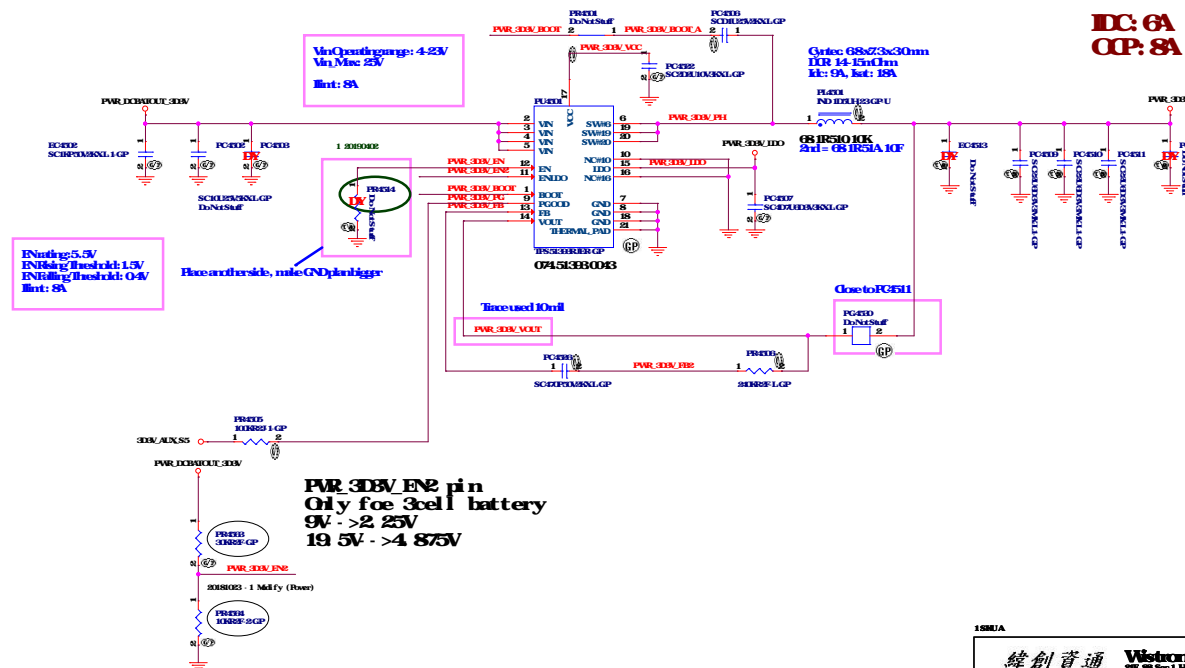
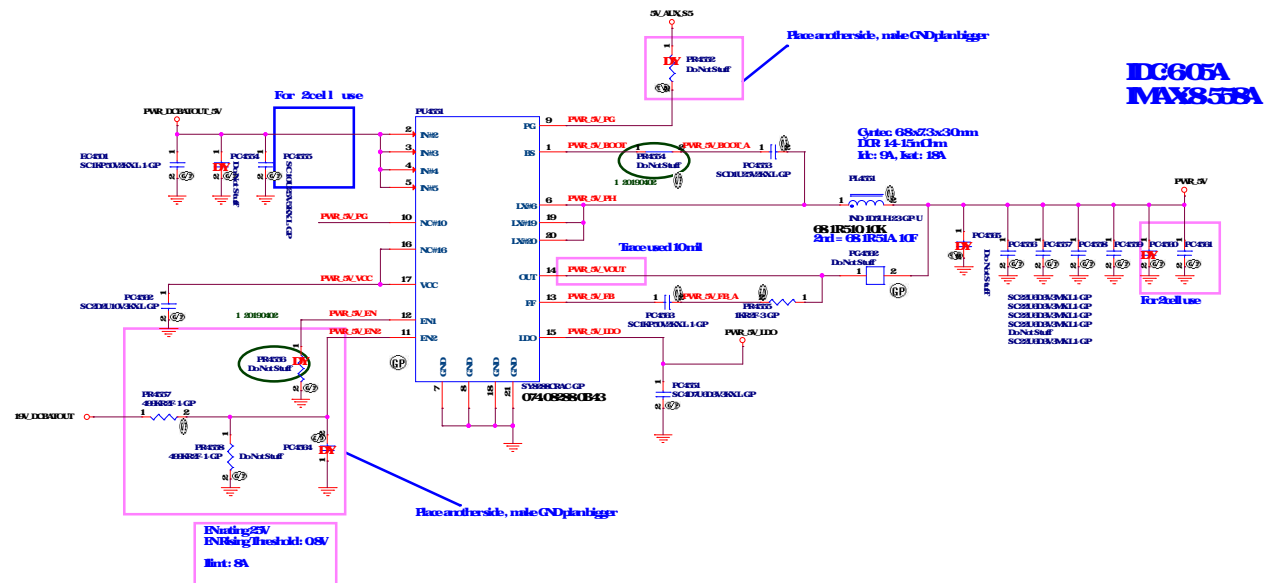
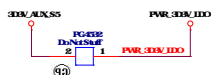
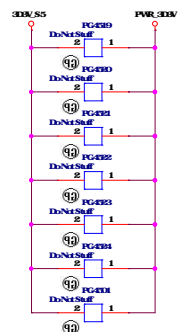


IADP: AC adapter detect current:
IADP: 20 or 40 x (Vsp - Vcn) / Rshdn

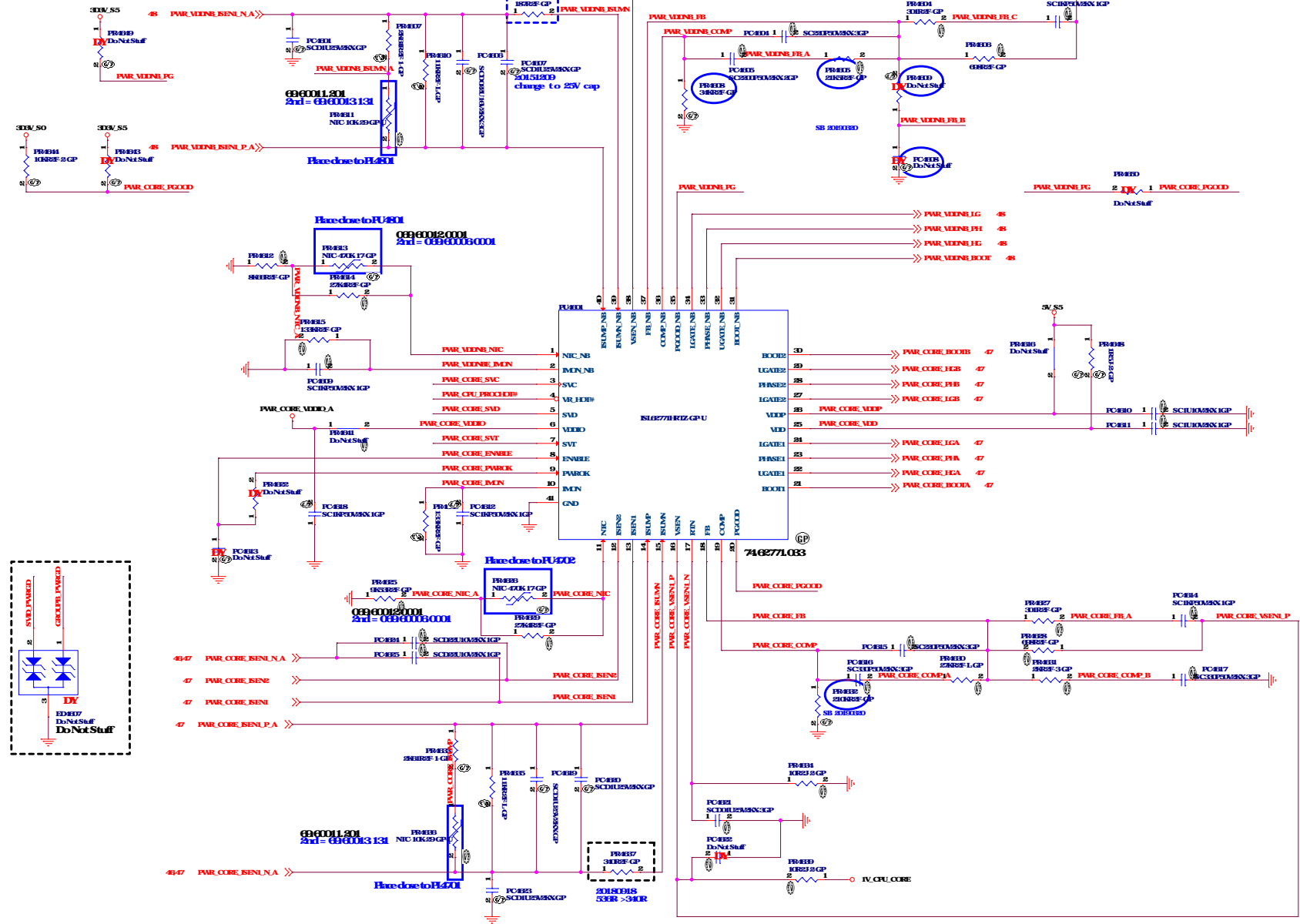
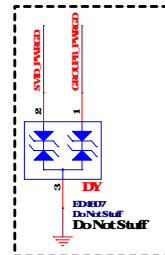
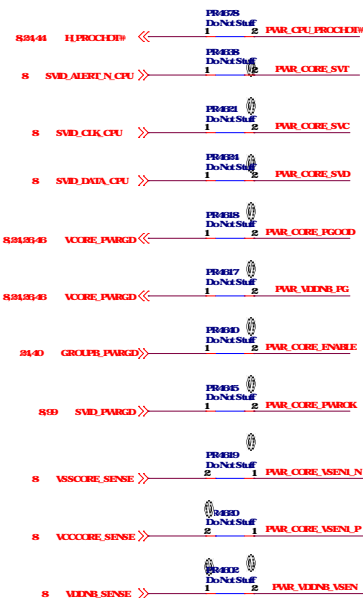
IDCHG: Discharge detect current:
= 8 or 16 x (Vsn - Vsp)



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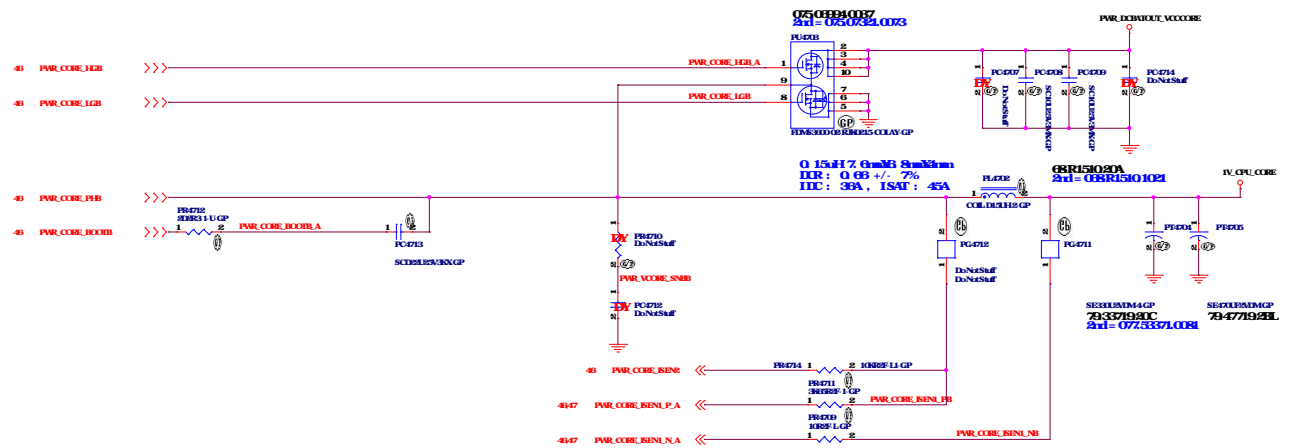
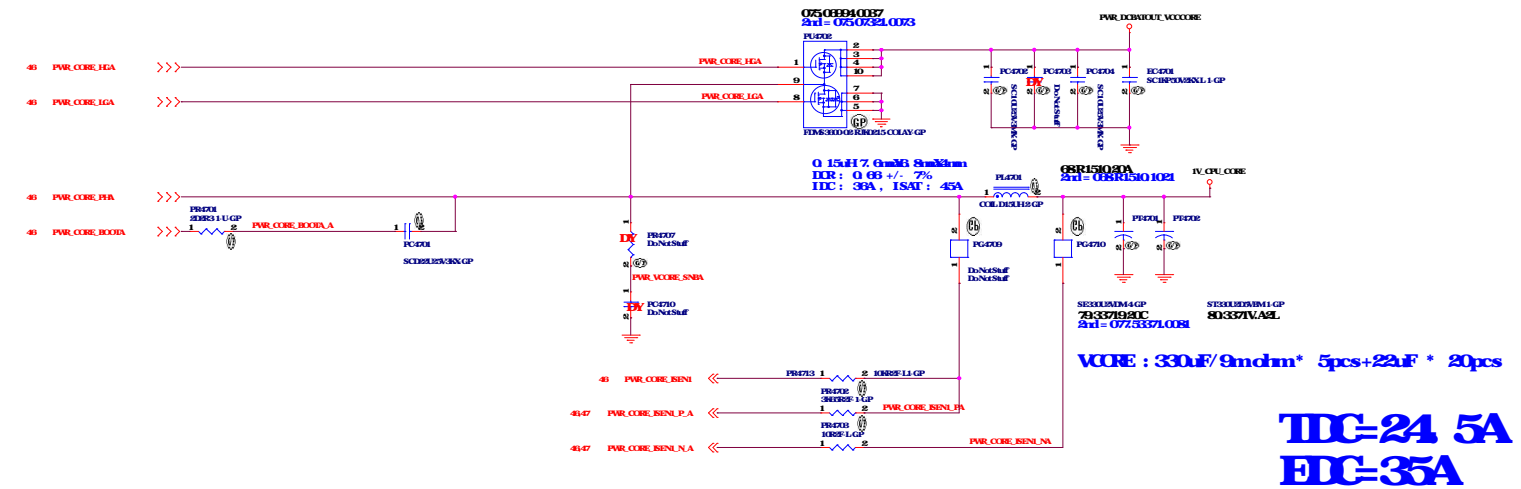
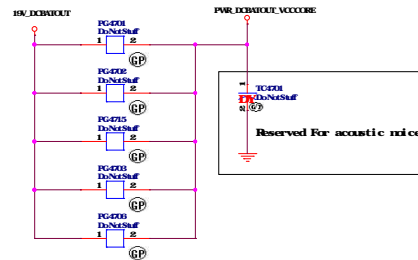


PWR_3DV_EN2 pin
Only for 3cell battery
9V - >2 25V
19 5V - >4 875V

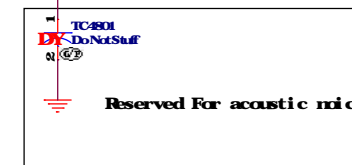
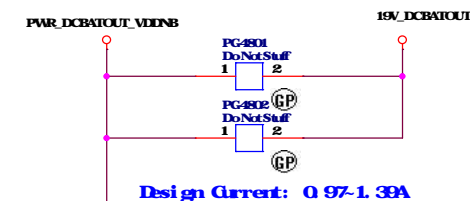
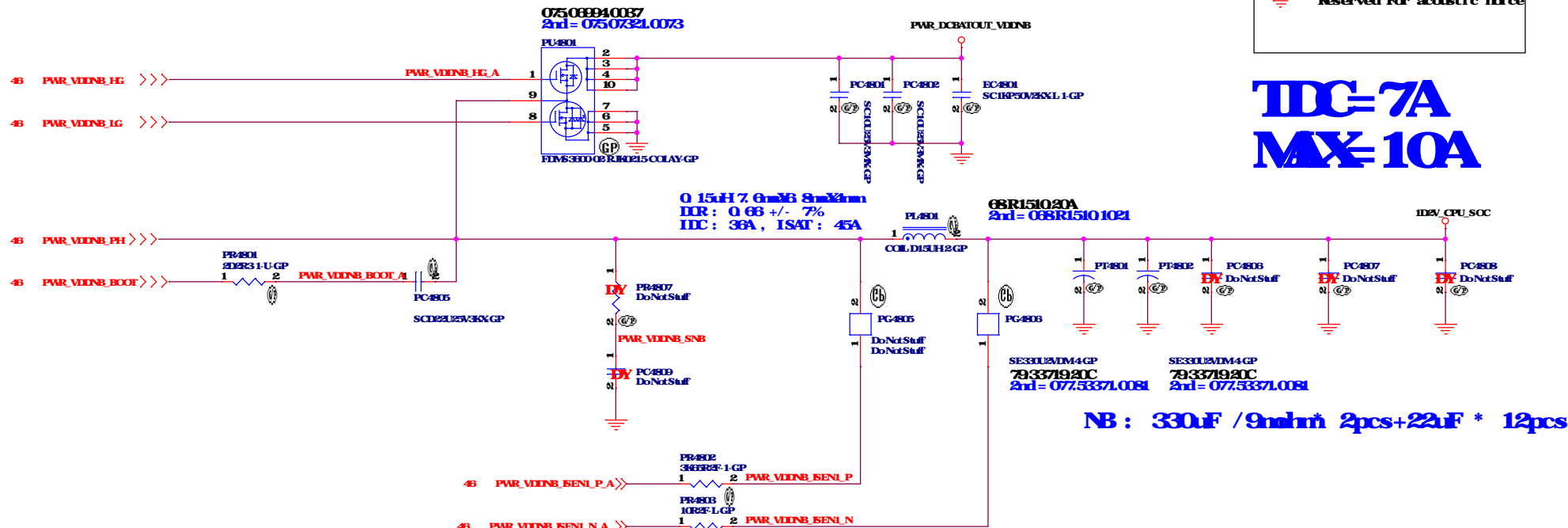
Min Func = APU VDDCR_VDD & VDDCR_SOC VR

Min Func = APU VDDOR_VDD 2ph HLS MsFET and Output LC

Design Current: 3 4-4 86A



Min Func = APU VDDR_SOC 1ph HLS MsFET and Output LC



IDC=7A
MAX=10A

1S80A

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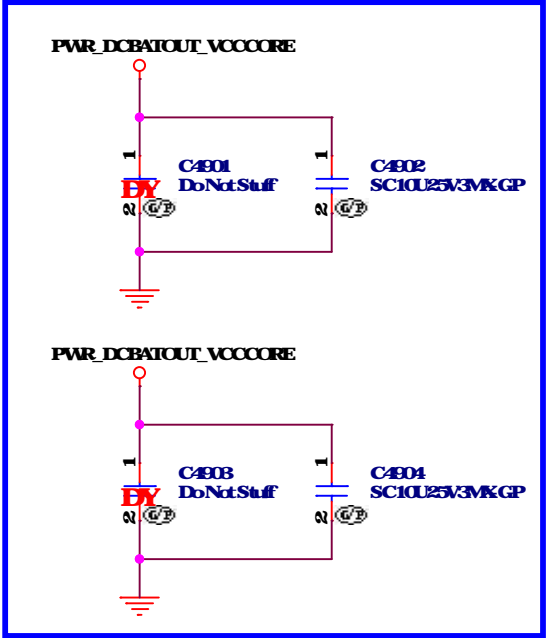
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APU VDDR_SOC VRMsFETs (33)

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Low Noise MCC



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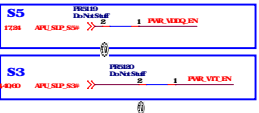
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Rev
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Date: Wednesday, April 17, 2009

Sheet 50 of 106

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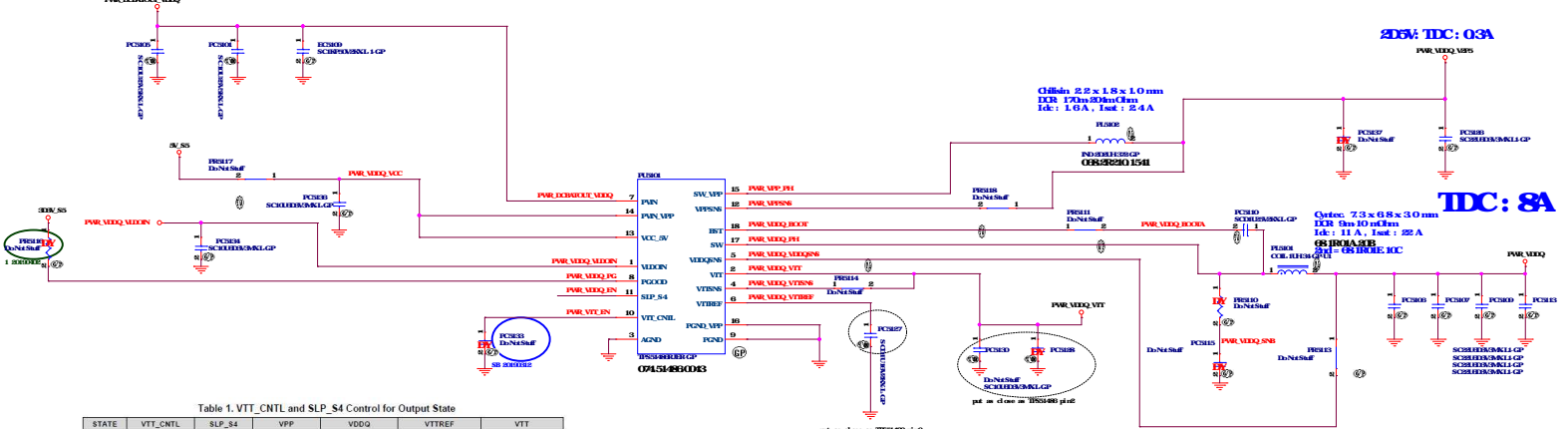
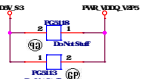
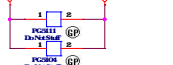
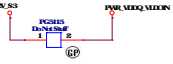
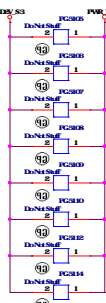
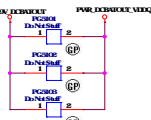
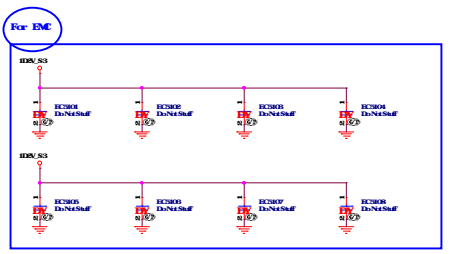


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VFP	VDDQ	VTTREF	VTT
S5	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	OFF (High-Z)	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

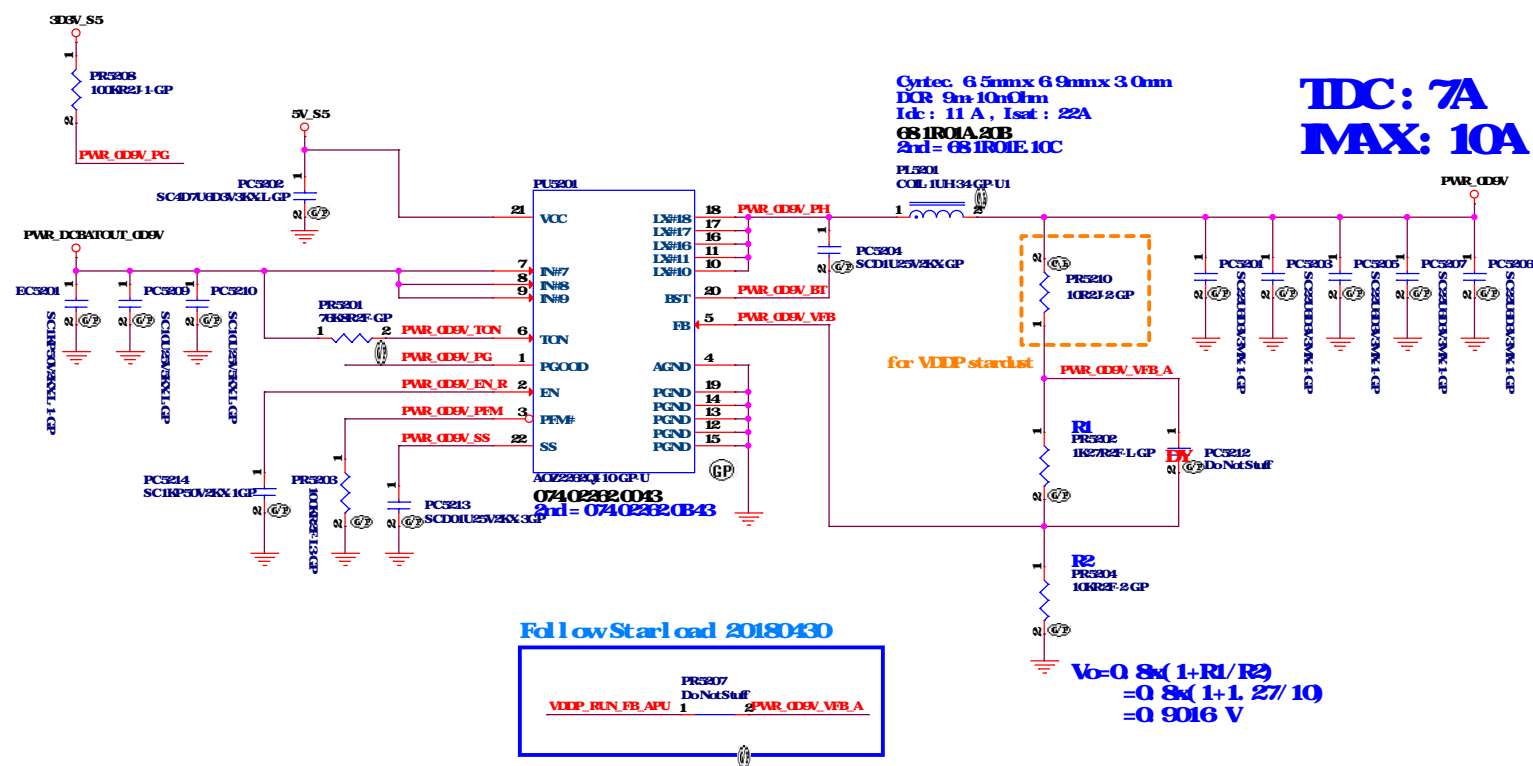


OFFPAGE GAP

IC COM	AO72262(10A) 074 02262 0043	AO72261(8A) 074 02261 0A73	AO72260(6A) 074 02260 0043
Clock	68 1R01A 20B 1IC : 10A	68 1R01A 20B 1IC : 10A	68 1R01A 20B 1IC : 10A
Output CAP	22uF/6 3V * 5pcs D* 1	22uF/6 3V * 4pcs D* 1	22uF/6 3V * 4pcs D* 1

AOZ2260 For OD9V

TDC: 7A
MAX: 10A



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POWER (AOZ2263Q_1D0V)

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Page: Wednesday, April 24, 2019 5:52 of 108

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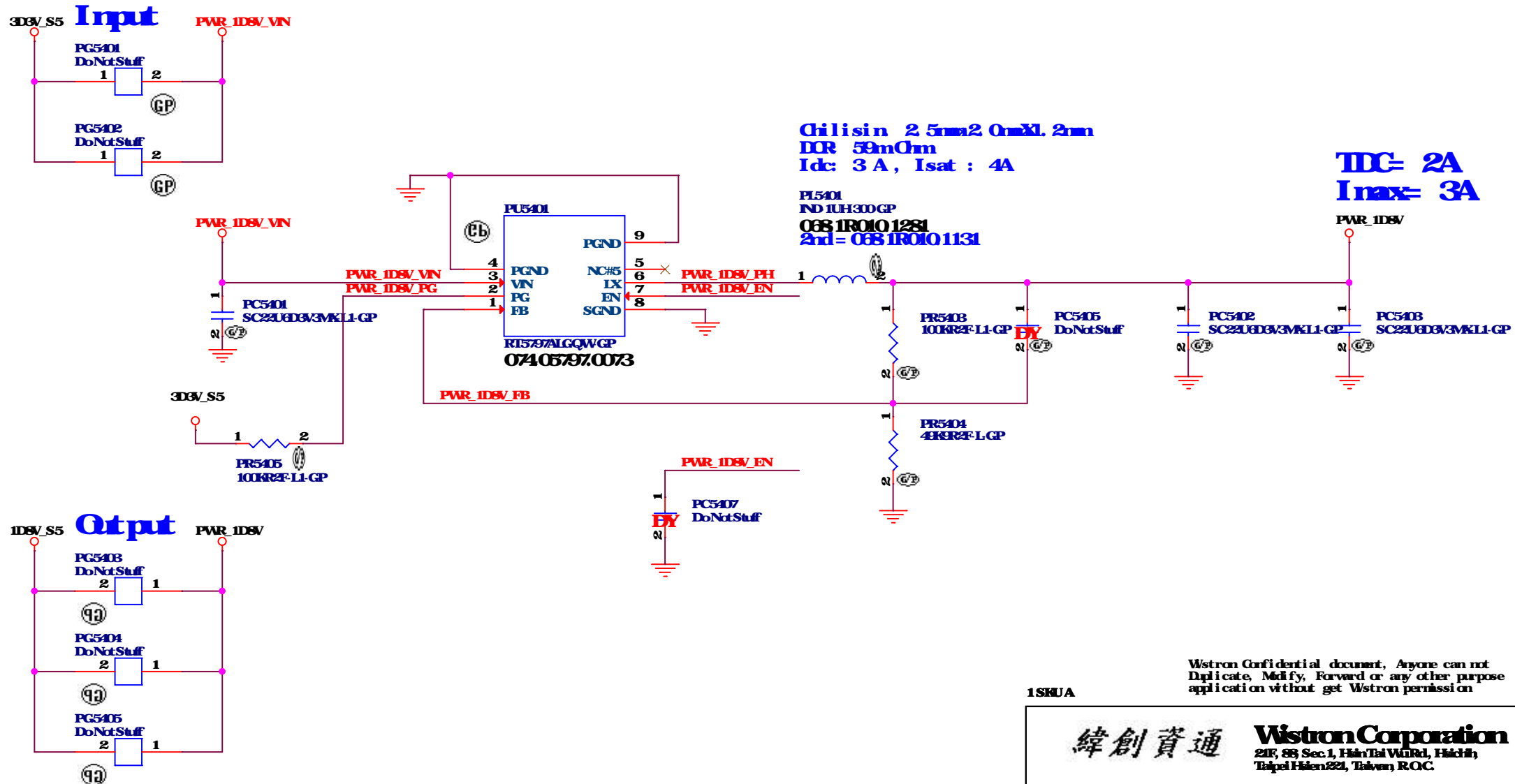
Date: Wednesday, April 17, 2009

Sheet 53 of 106

SSID = PWR Plane, Regulator_1DSV

1745 3V_5V_PWRGD
52 PWR_1DSV_PG

1 2 PWR_1DSV_EN
PR5465
DoNotStuff



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Power(RI579/ALGQW_1DSV)		
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Page 35 of 108

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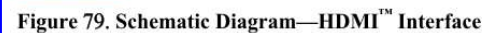
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HDMI CONNECTOR



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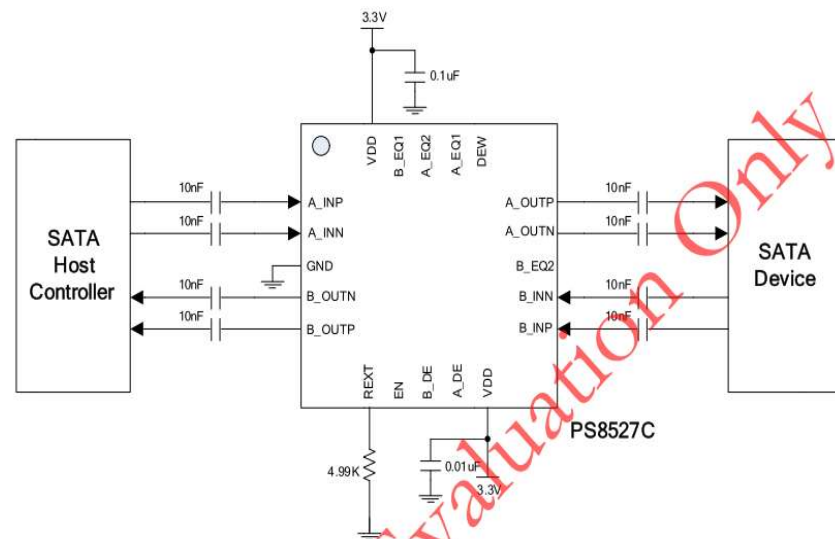
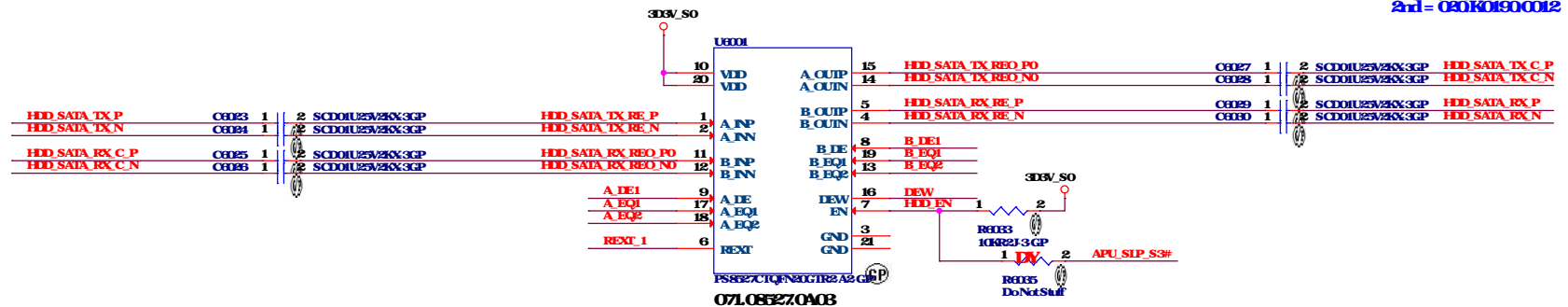
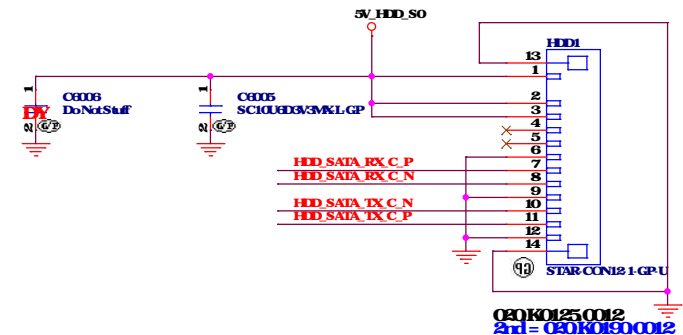
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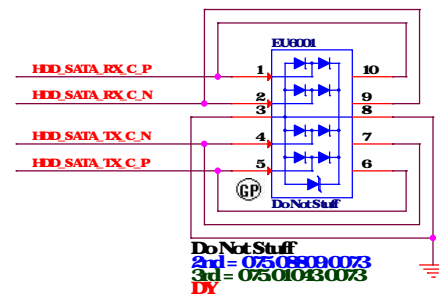
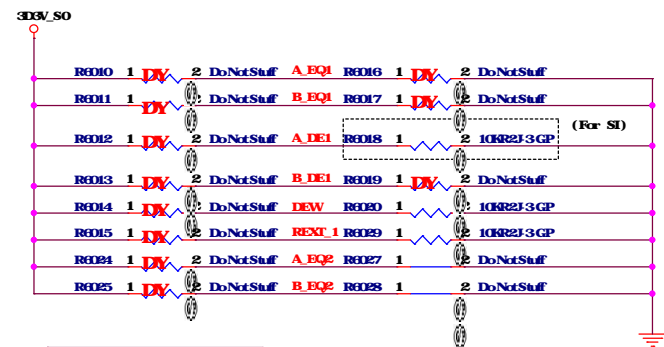
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Display (RSVD)					
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Date	Wednesday, April 17, 2019			Sheet	59 of 106

17,24,40,51 APU_SLP_S3#

SATA HDD Connector



9	A_DE	I	Programmable output de-emphasis level setting for channel A.	
			Internally tied to VDD/2(M status).	
			A_DE	De_Emphasis
			M	-3.5dB(Default)
			L	0dB
			H	-6dB

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NTIO(HDD)

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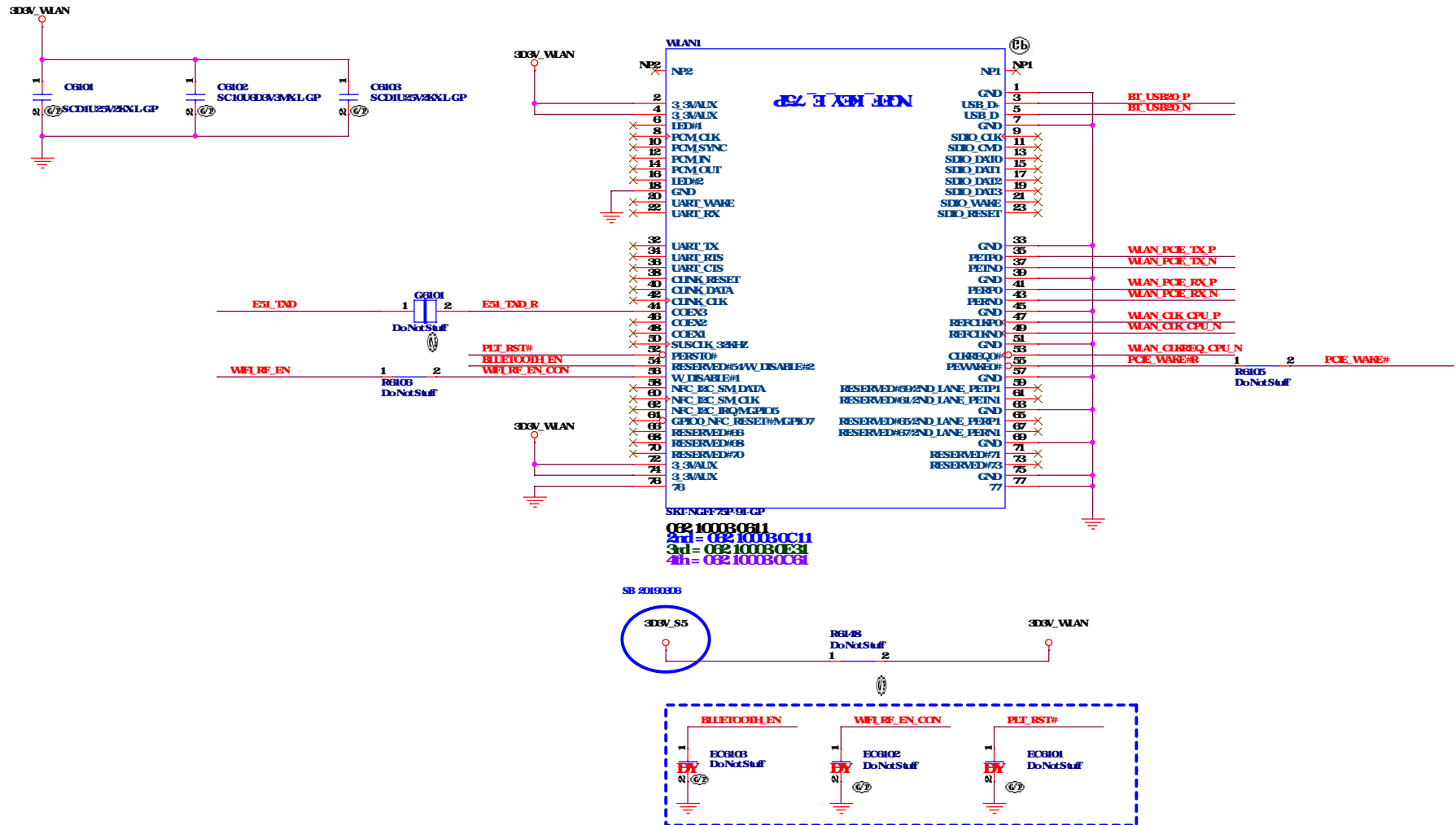
Number	Rev
Strongbow_PK	1

Date: Wednesday, April 17, 2019

Sheet 60 of 108

SSID = Wreless Mni Card Connector(802 11a/b/g/n)

2468 ESI_TMD >>>
 1763887689 PLT_RST# >>>
 178489 BLUETOOTH_EN >>>
 24 WIRELESS_EN >>>
 89 WIRELESS_EN_CON >>>
 3889 BT_USB20_P >>>
 3889 BT_USB20_N >>>
 389 WLAN_PCE_TX_P >>>
 389 WLAN_PCE_TX_N >>>
 389 WLAN_PCE_RX_P >>>
 389 WLAN_PCE_RX_N >>>
 1689 WLAN_CLK_CPU_P >>>
 1689 WLAN_CLK_CPU_N >>>
 176389 PCE_WAKE# <<<
 1689 WLAN_CLKREQ_CPU_N <<<



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1

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Sheet 02 of 106

SSID = M2

176L89 PCIE_WAKE# <<>>
16 SSD_CLKREQ_CPU_N <<>>
176L887889 PLT_RST# <<>>
17 DEVSIP <<>>

16 SSD_CLK_CPU_P <<>>
16 SSD_CLK_CPU_N <<>>

M2 SSD (SATA)

3 SSD_SATA_RX_N <<>>
3 SSD_SATA_RX_P <<>>

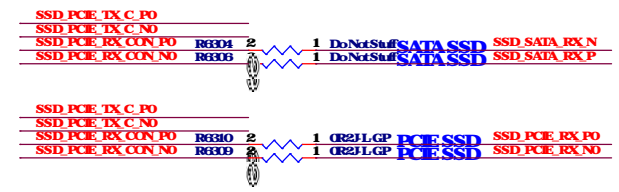
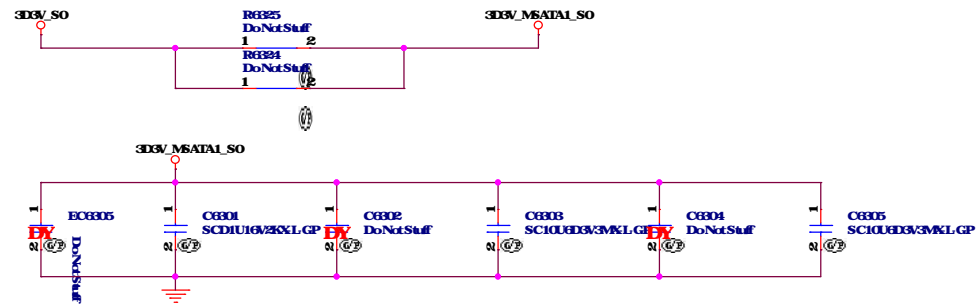
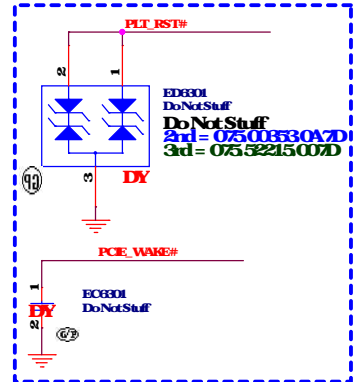
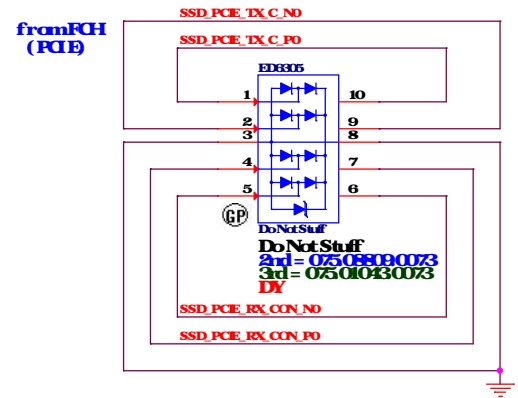
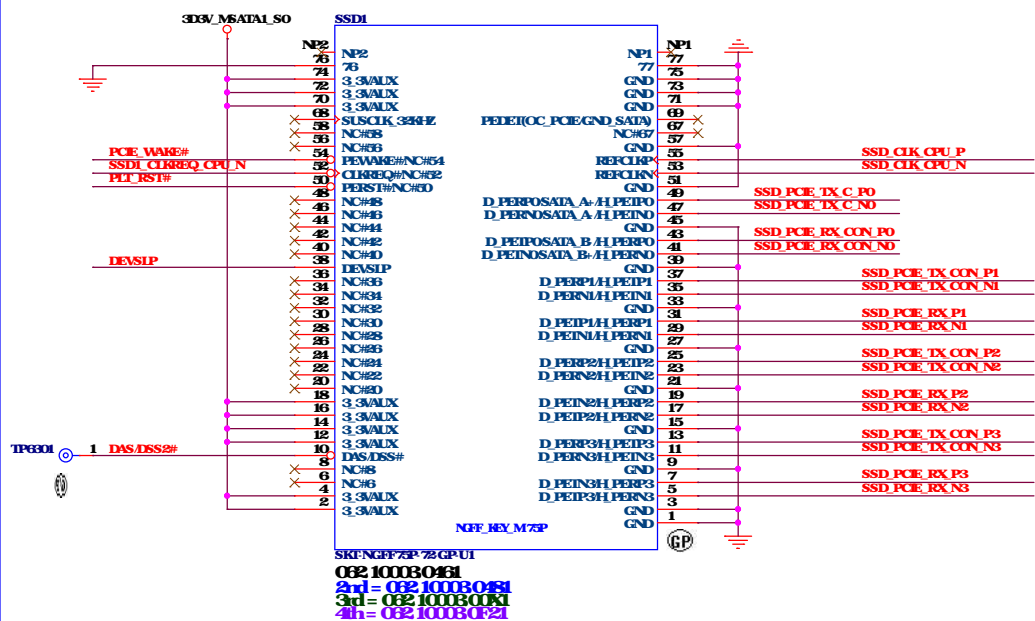
M2 SSD (PCIe)

3 SSD_PCE_RX_P0 <<>>
3 SSD_PCE_RX_N0 <<>>

3 SSD_PCE_TX_CON_P1 <<>>
3 SSD_PCE_TX_CON_N1 <<>>
3 SSD_PCE_RX_P1 <<>>
3 SSD_PCE_RX_N1 <<>>

3 SSD_PCE_TX_CON_P2 <<>>
3 SSD_PCE_TX_CON_N2 <<>>
3 SSD_PCE_RX_P2 <<>>
3 SSD_PCE_RX_N2 <<>>

3 SSD_PCE_TX_CON_P3 <<>>
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3 SSD_PCE_RX_P3 <<>>
3 SSD_PCE_RX_N3 <<>>



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Title

LED / Button / Power Button

Size
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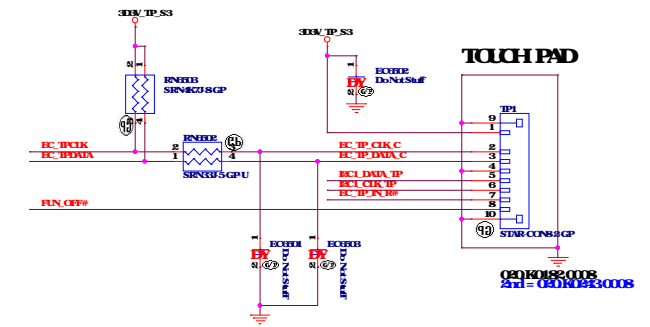
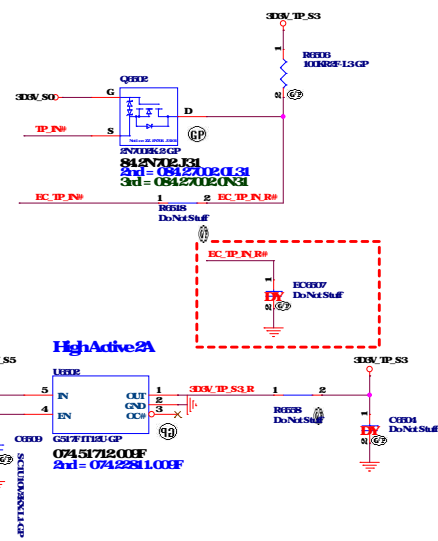
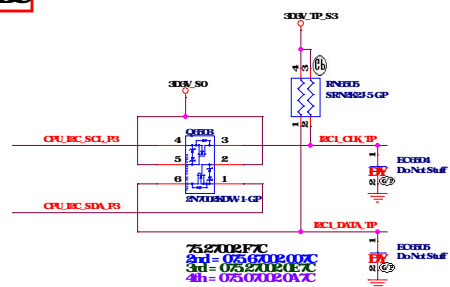
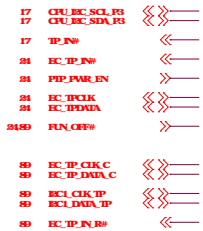
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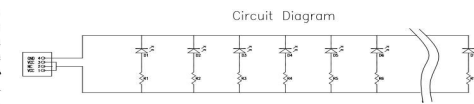
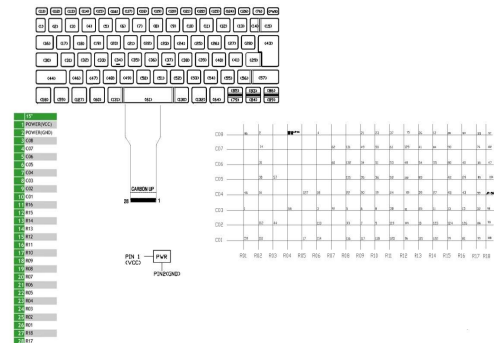
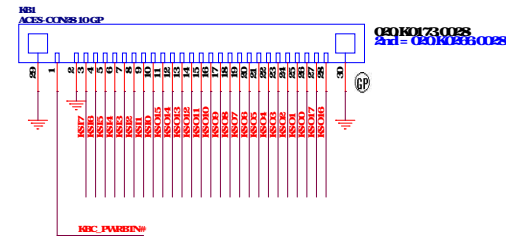
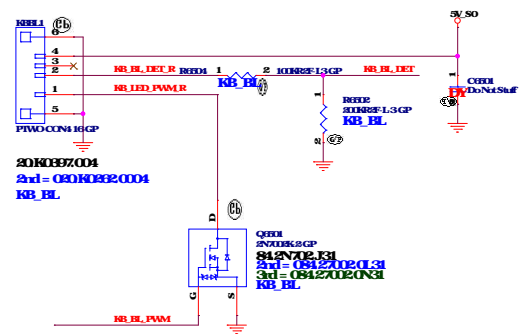
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Sheet 01 of 106



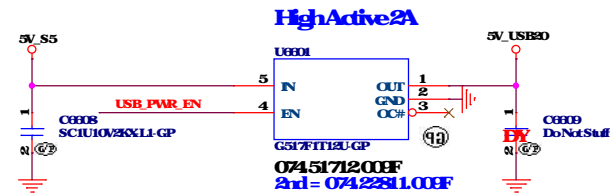
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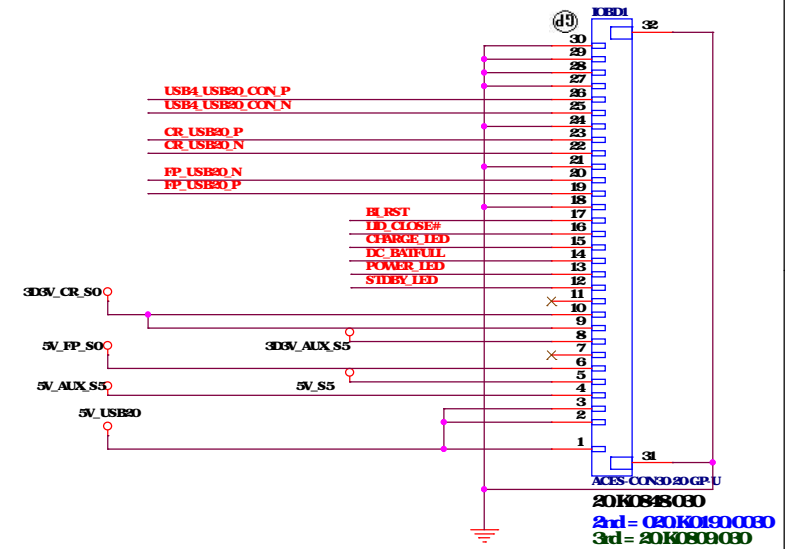
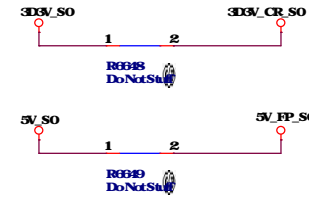
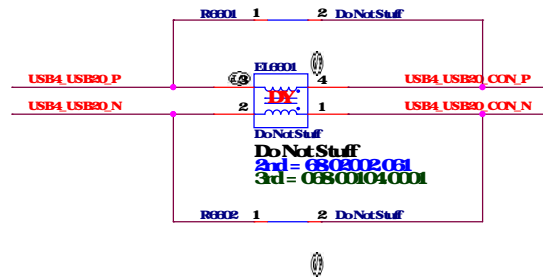
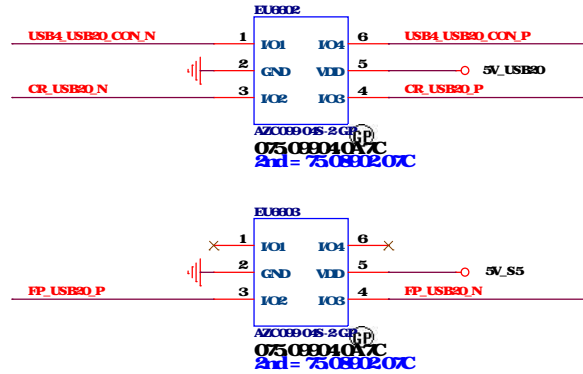
SSID = User. Interface

2435 USB_PWR_EN >>>
 1848 USB4_USB20_P <<<
 1848 USB4_USB20_N <<<
 3848 CR_USB20_P <<<
 3848 CR_USB20_N <<<
 3848 FP_USB20_N <<<
 3848 FP_USB20_P <<<
 4348 BL_RST <<<
 2489 LID_CLOSE# <<<
 2489 CHARGE_LED >>>
 2489 DC_BATFULL >>>
 2489 POWER_LED >>>
 2489 STDBY_LED >>>

3D3V_CR_S0 <<<
 3D3V_AUX_S5 <<<
 5V_FP_S0 <<<
 5V_S5 <<<
 5V_AUX_S5 <<<
 5V_USB20 <<<
 80 USB4_USB20_CON_P <<<
 80 USB4_USB20_CON_N <<<



Close connector



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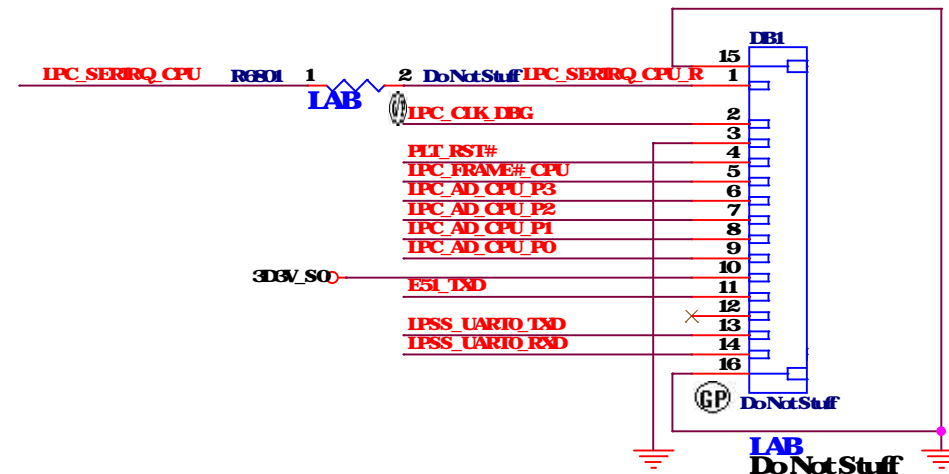
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Rev
1

Date: Wednesday, April 17, 2009

Sheet 67 of 106

1624 IPC_SERIRQ_CPU <<>>—
16 IPC_CLK_DBG >>—
1761,63,76,89 PLT_RST# >>—
1624 IPC_FRAME#_CPU <<>>—
1624 IPC_AD_CPU_P3 <<>>—
1624 IPC_AD_CPU_P2 <<>>—
1624 IPC_AD_CPU_P1 <<>>—
1624 IPC_AD_CPU_P0 <<>>—
2461 E5U_TXD >>—
16 IPSS_UART0_TXD >>—
16 IPSS_UART0_RXD >>—



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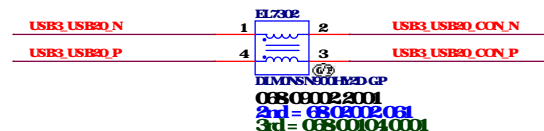
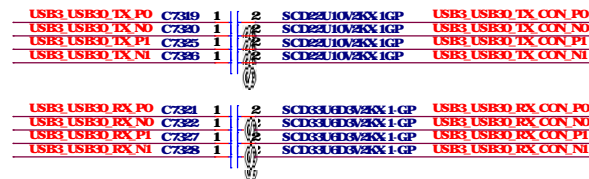
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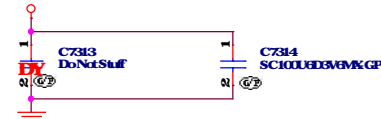
Sheet 71 of 108

USB HOST

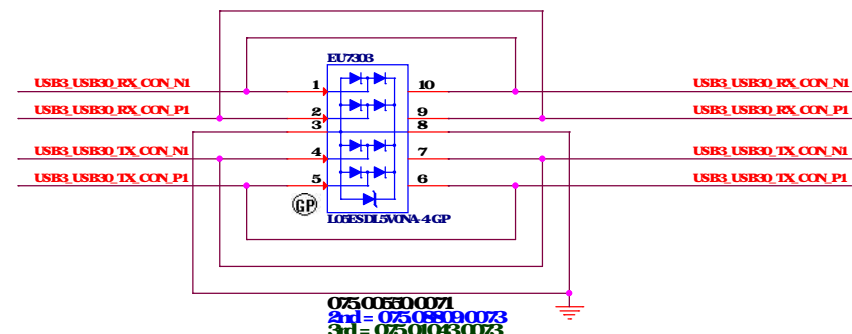
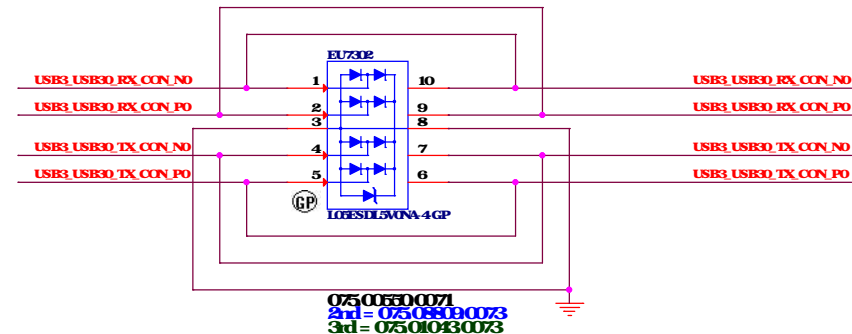
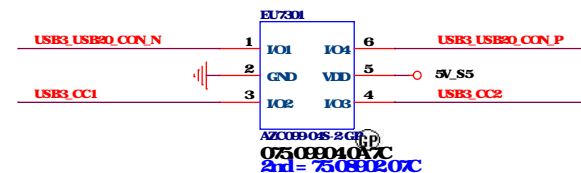
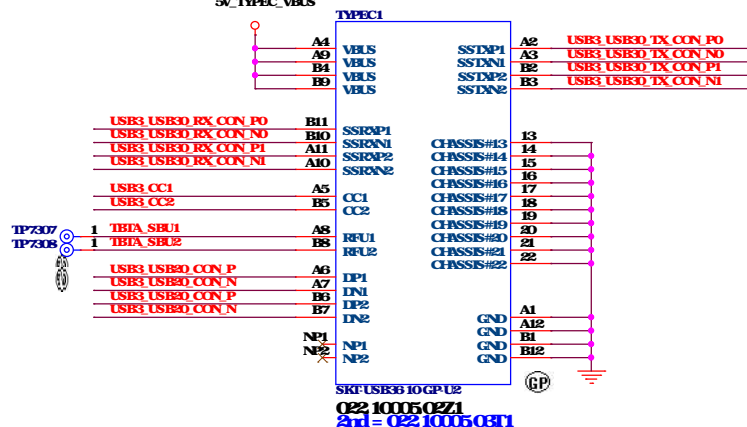
18 USB3_USB20_N
18 USB3_USB20_P
18 USB3_USB20_TX_PO
18 USB3_USB20_TX_NO
18 USB3_USB20_RX_PO
18 USB3_USB20_RX_NO
18 USB3_USB20_TX_PI
18 USB3_USB20_TX_NI
18 USB3_USB20_RX_PI
18 USB3_USB20_RX_NI
80 USB3_USB20_CON_P
80 USB3_USB20_CON_N
72,80 USB3_CC1
72,80 USB3_CC2



5V_TYPEC_VBUS



5V_TYPEC_VBUS



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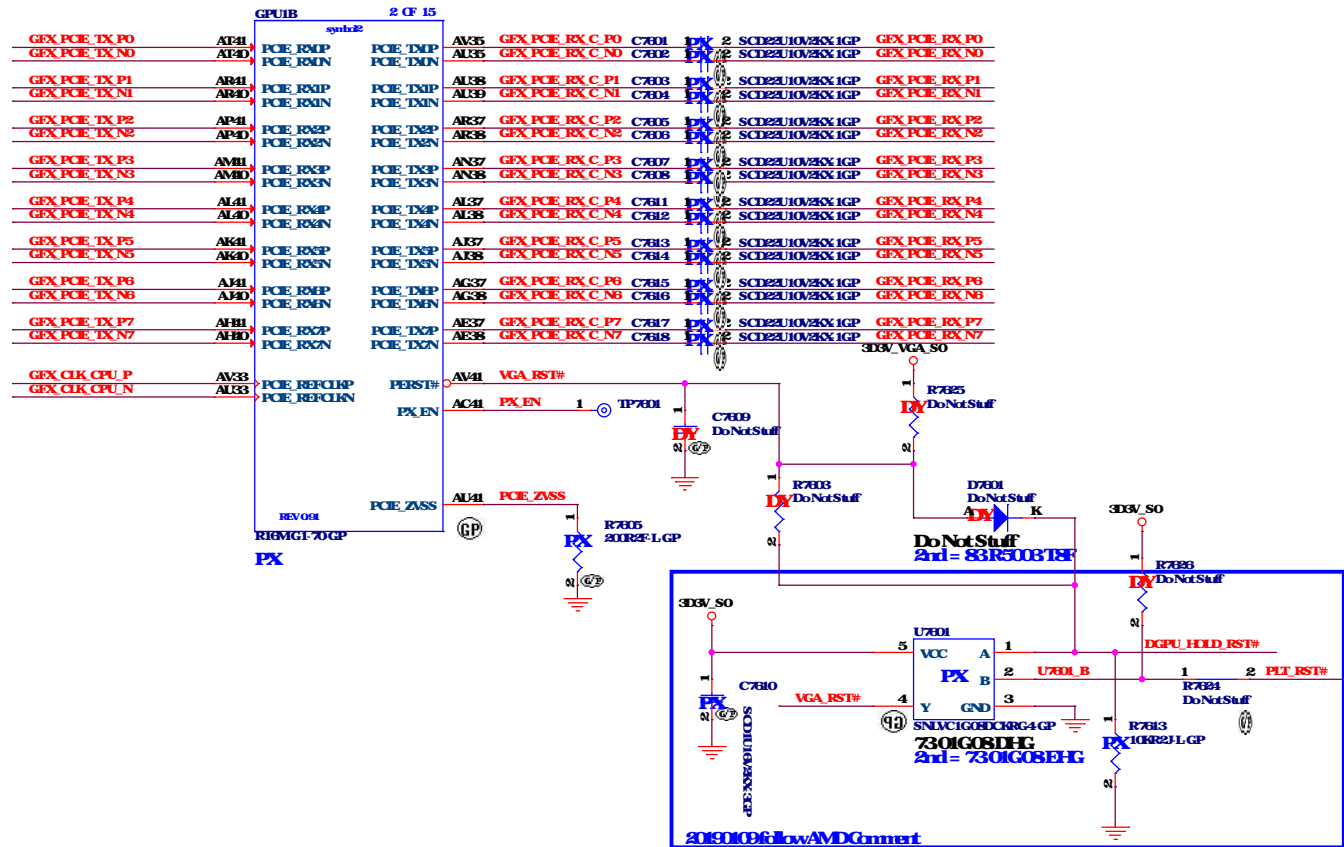
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1

Date: Wednesday, April 17, 2009

Sheet 75 of 106

Min Func = dGPU

3	GFX_PCE_TX_P0	>>>
3	GFX_PCE_TX_N0	>>>
3	GFX_PCE_TX_P1	>>>
3	GFX_PCE_TX_N1	>>>
3	GFX_PCE_TX_P2	>>>
3	GFX_PCE_TX_N2	>>>
3	GFX_PCE_TX_P3	>>>
3	GFX_PCE_TX_N3	>>>
3	GFX_PCE_RX_P0	<<<
3	GFX_PCE_RX_N0	<<<
3	GFX_PCE_RX_P1	<<<
3	GFX_PCE_RX_N1	<<<
3	GFX_PCE_RX_P2	<<<
3	GFX_PCE_RX_N2	<<<
3	GFX_PCE_RX_P3	<<<
3	GFX_PCE_RX_N3	<<<
16	GFX_CLK_CPU_P	>>>
16	GFX_CLK_CPU_N	>>>
16	DGPU_HOLD_RST#	>>>
70,63,68,81	PLT_RST#	>>>
85	VGA_RST#	<<<
3	GFX_PCE_TX_P4	>>>
3	GFX_PCE_TX_N4	>>>
3	GFX_PCE_TX_P5	>>>
3	GFX_PCE_TX_N5	>>>
3	GFX_PCE_TX_P6	>>>
3	GFX_PCE_TX_N6	>>>
3	GFX_PCE_TX_P7	>>>
3	GFX_PCE_TX_N7	>>>
3	GFX_PCE_RX_P4	<<<
3	GFX_PCE_RX_N4	<<<
3	GFX_PCE_RX_P5	<<<
3	GFX_PCE_RX_N5	<<<
3	GFX_PCE_RX_P6	<<<
3	GFX_PCE_RX_N6	<<<
3	GFX_PCE_RX_P7	<<<
3	GFX_PCE_RX_N7	<<<

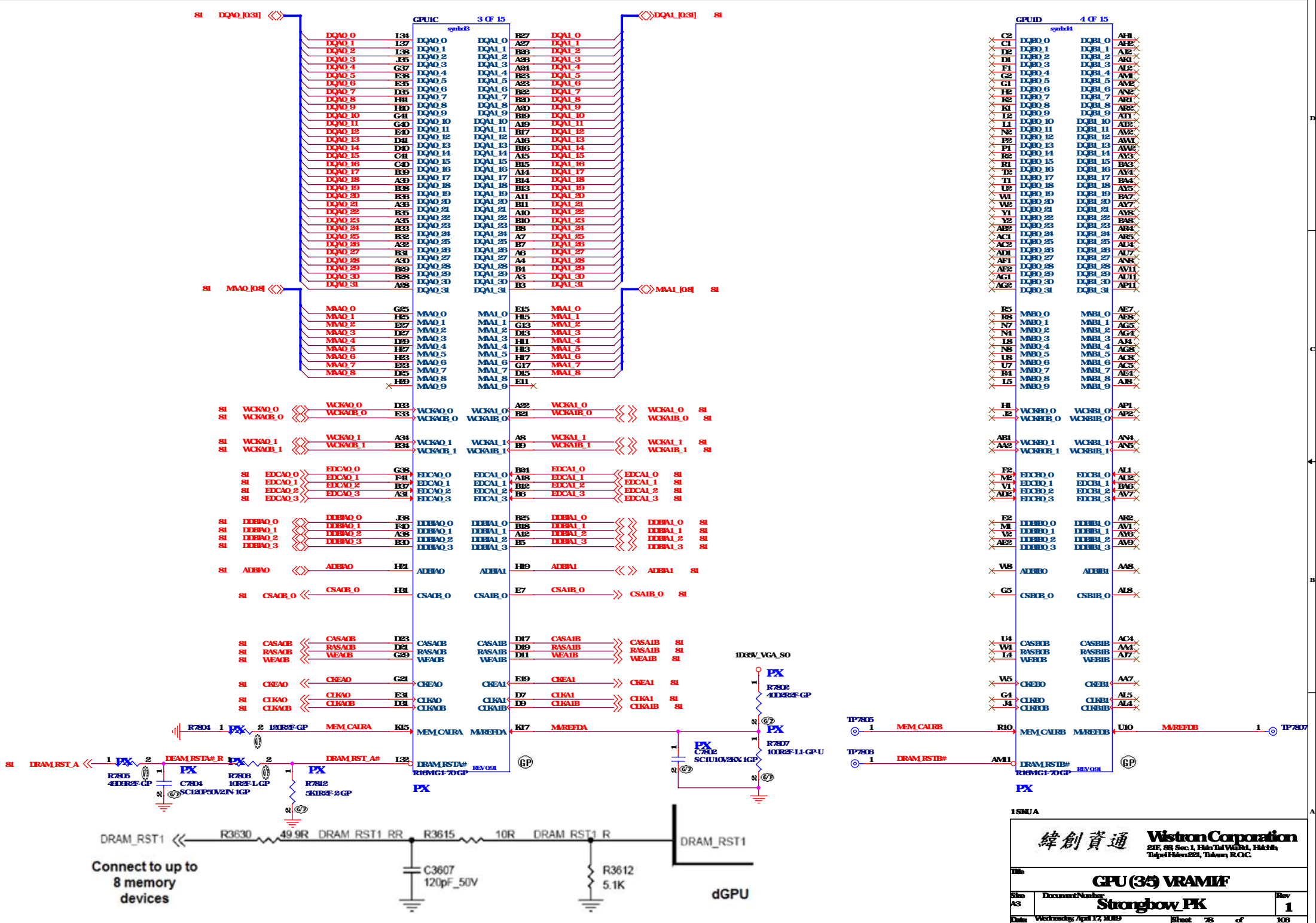


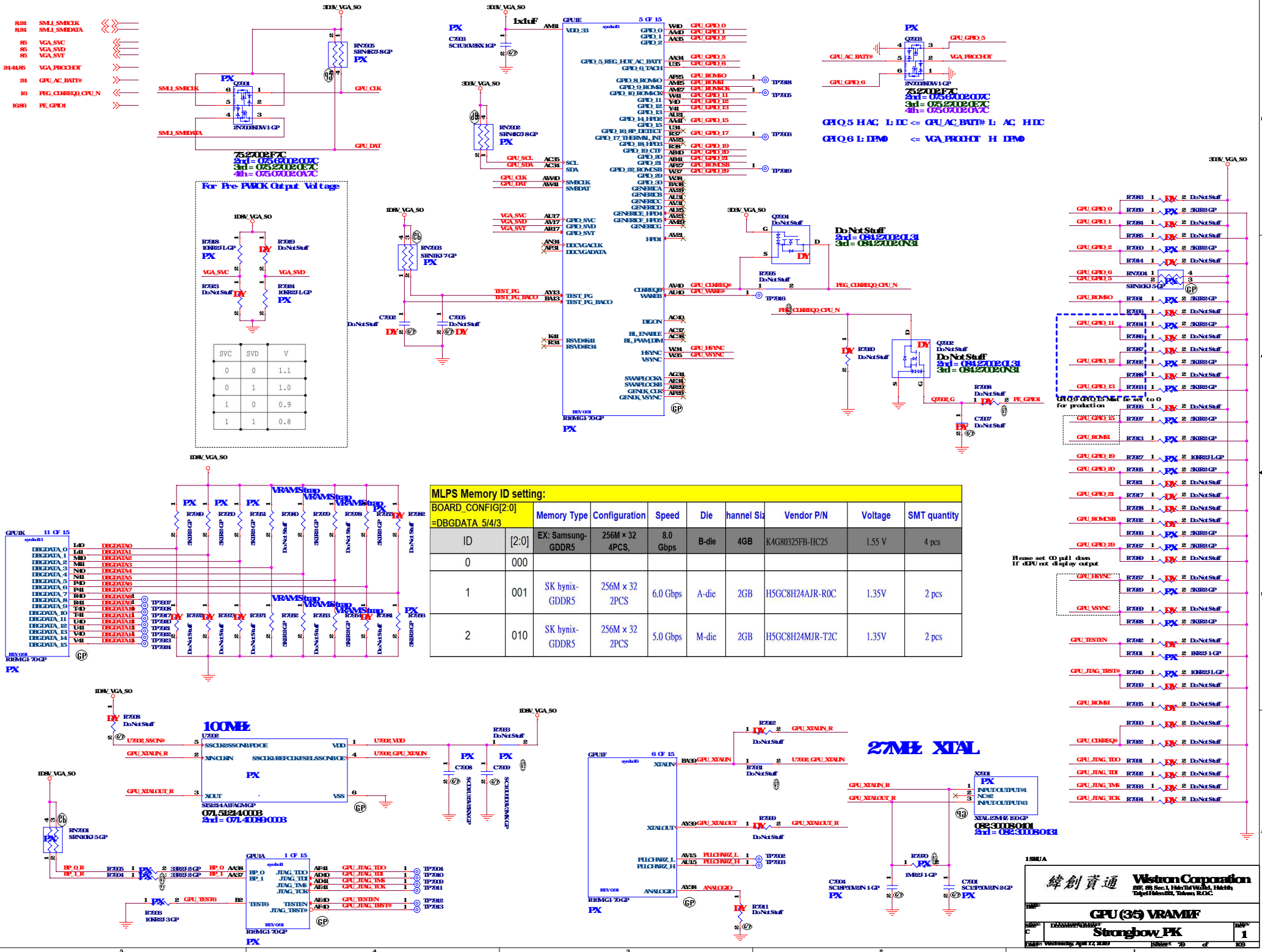
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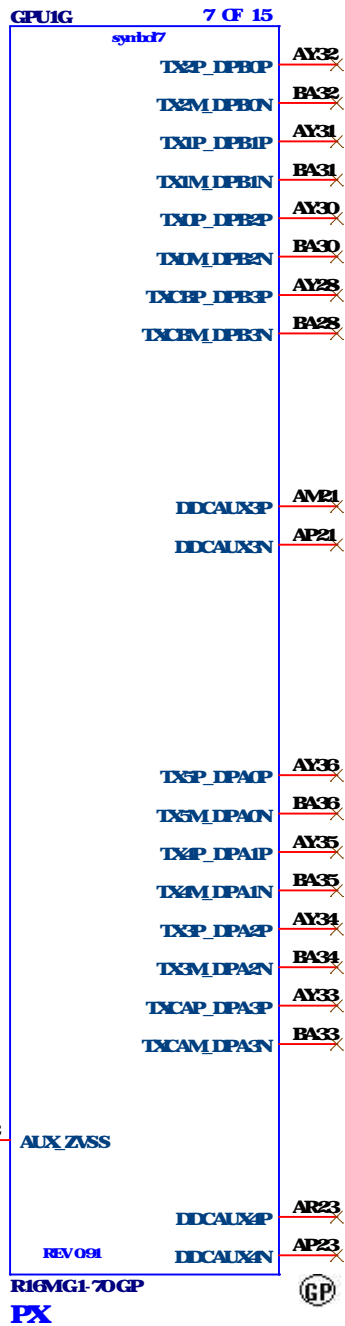
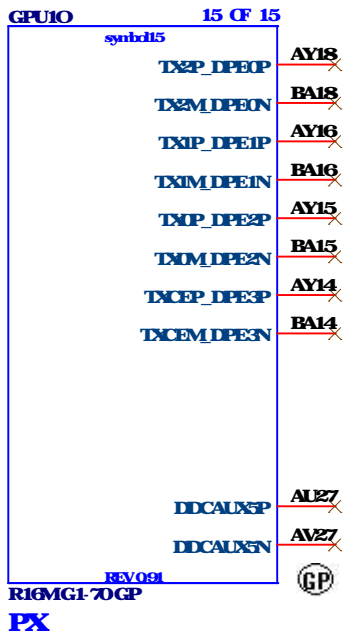
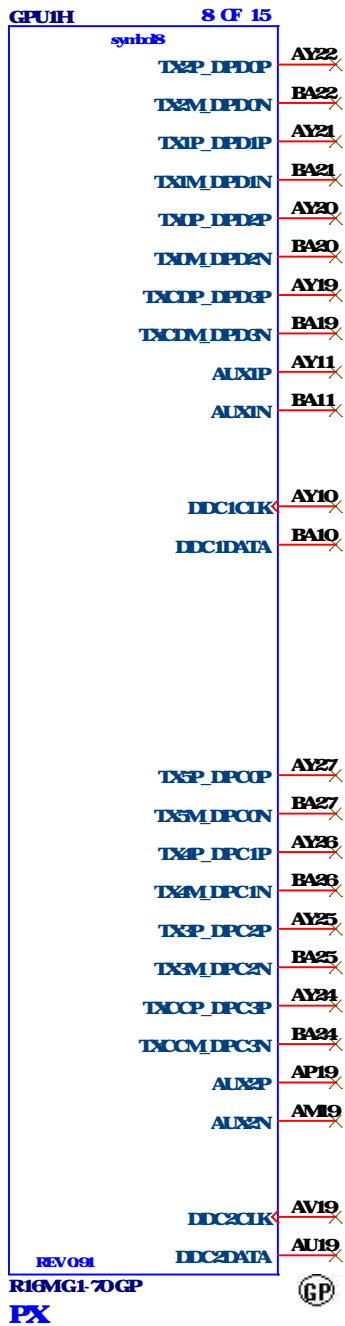
1580A

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GPU (1/5) PEG		
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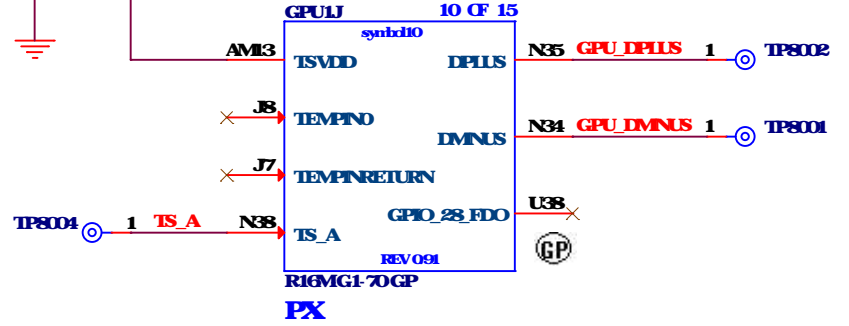




1x1uF

ID6V_VGA_S0

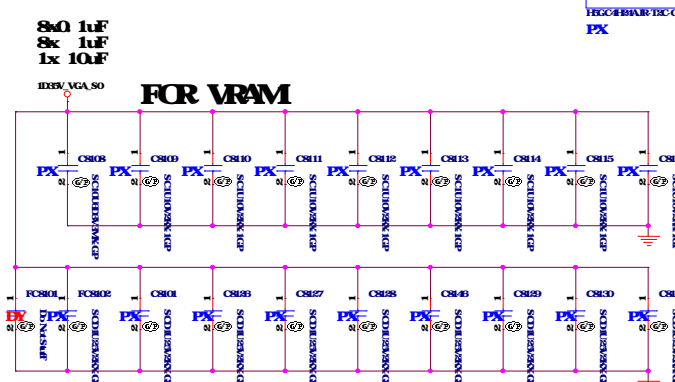
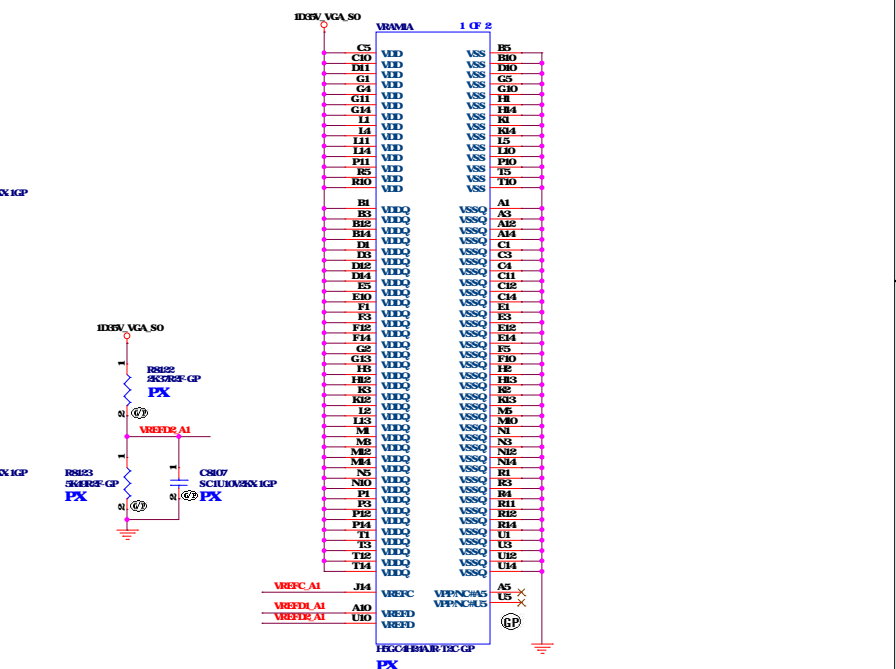
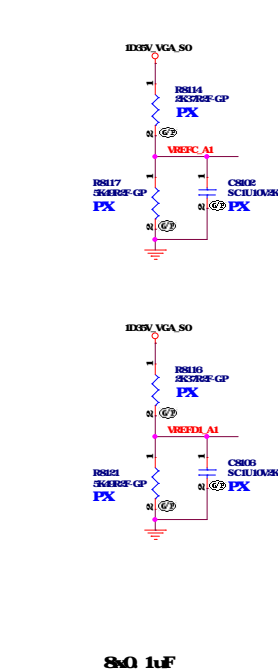
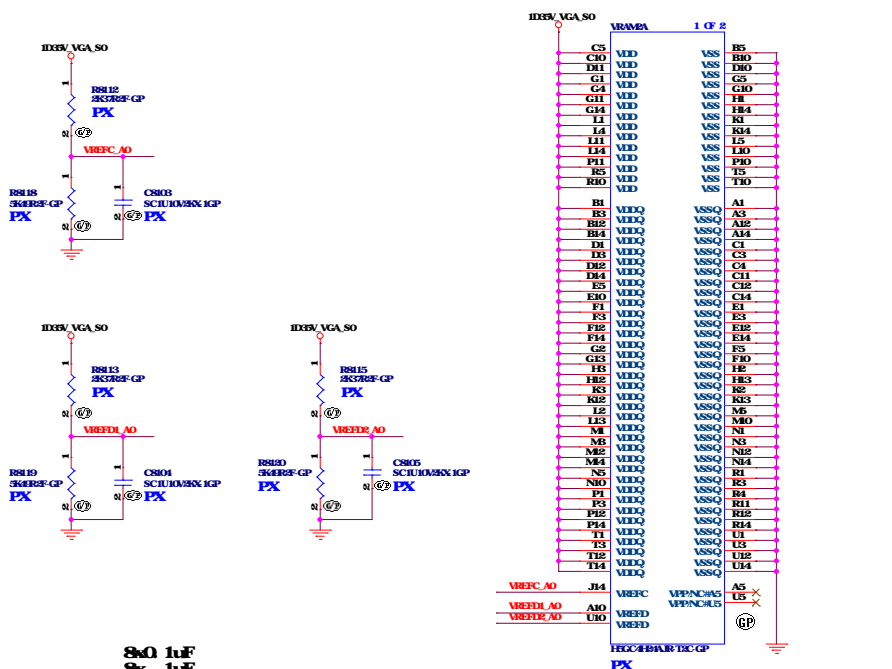
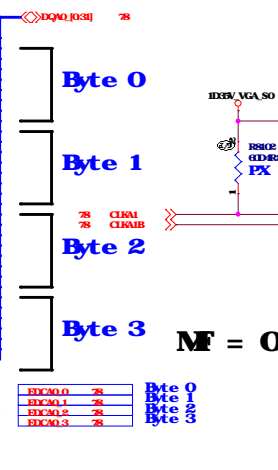
C8001
SCI10V2KX1GP
PX



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<p>Size A4</p>	<p>Document Number Strongbow_PK</p>
<p>Date Wednesday, April 17, 2019</p>	<p>Rev 1</p>
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Sheet 82 of 106

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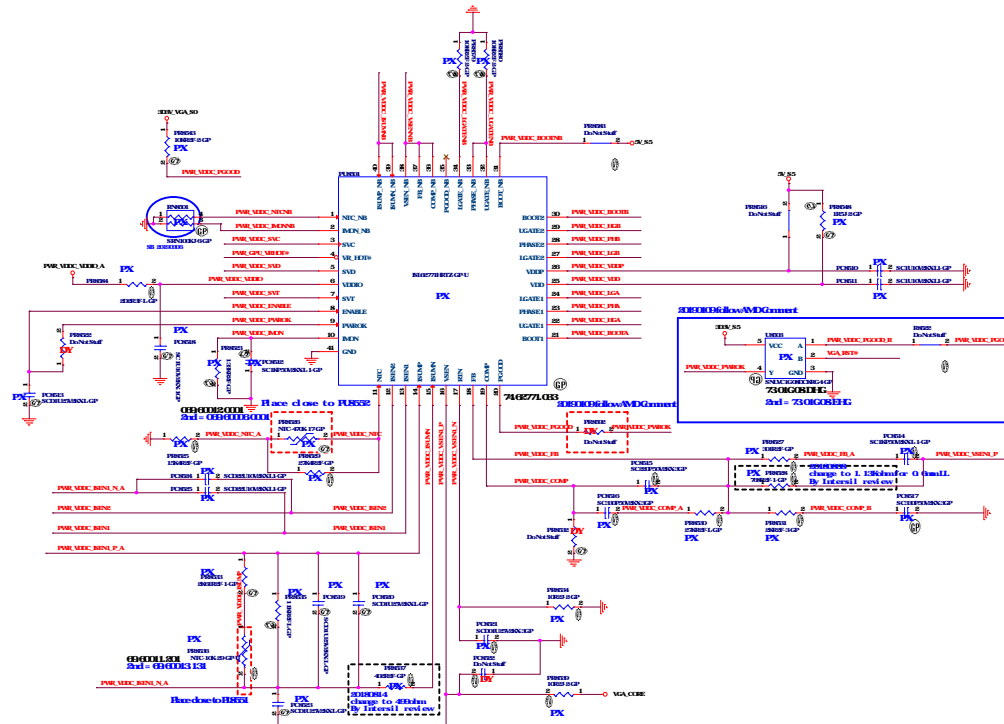
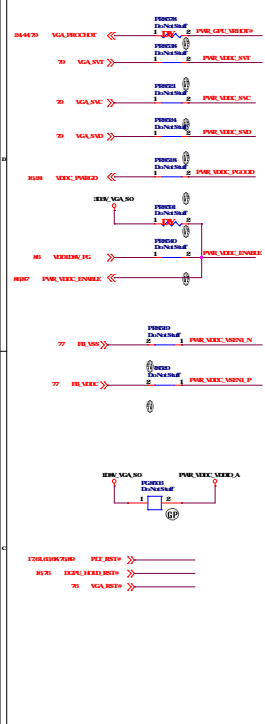
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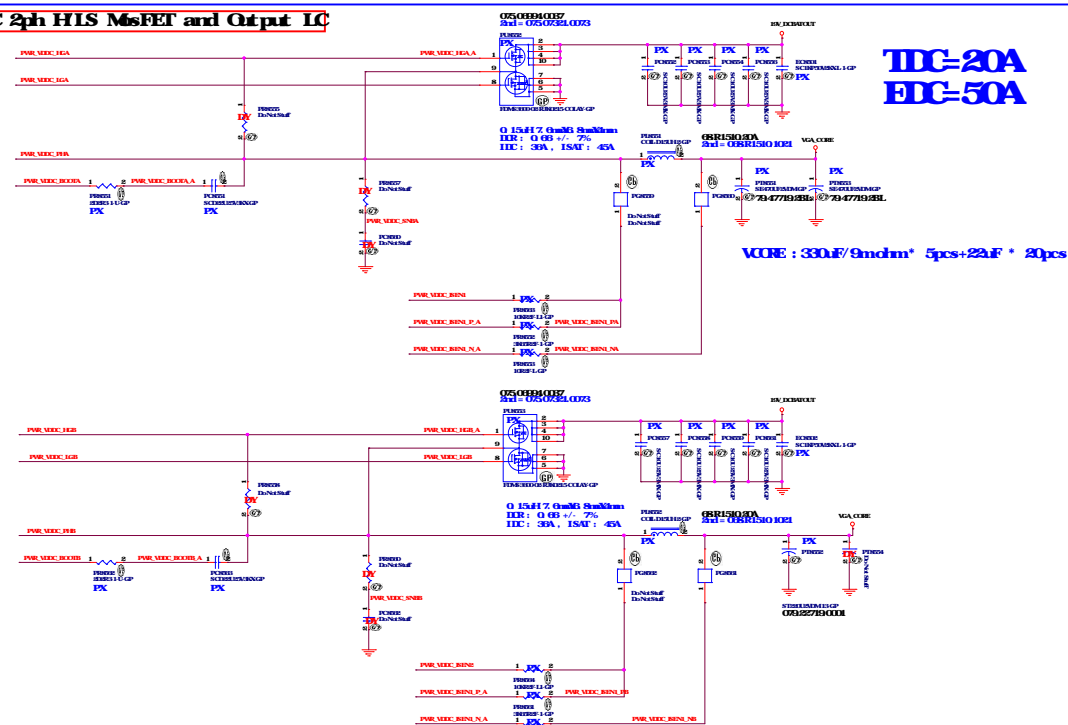
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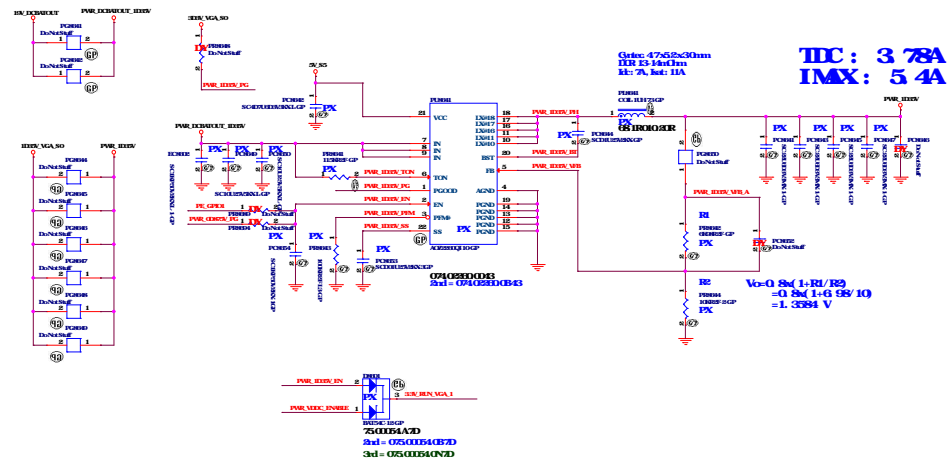
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Sheet 84 of 106

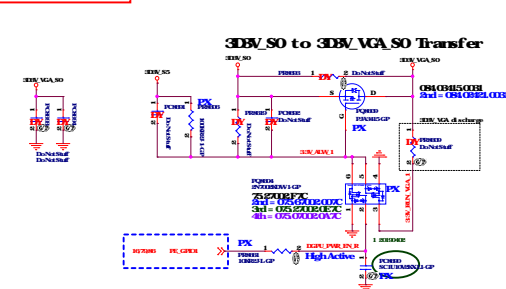
$$\text{Min Func} = \text{GPU VDC VR}$$


Min Func = GPU VDDC 2ph HLS MisFET and Output LC



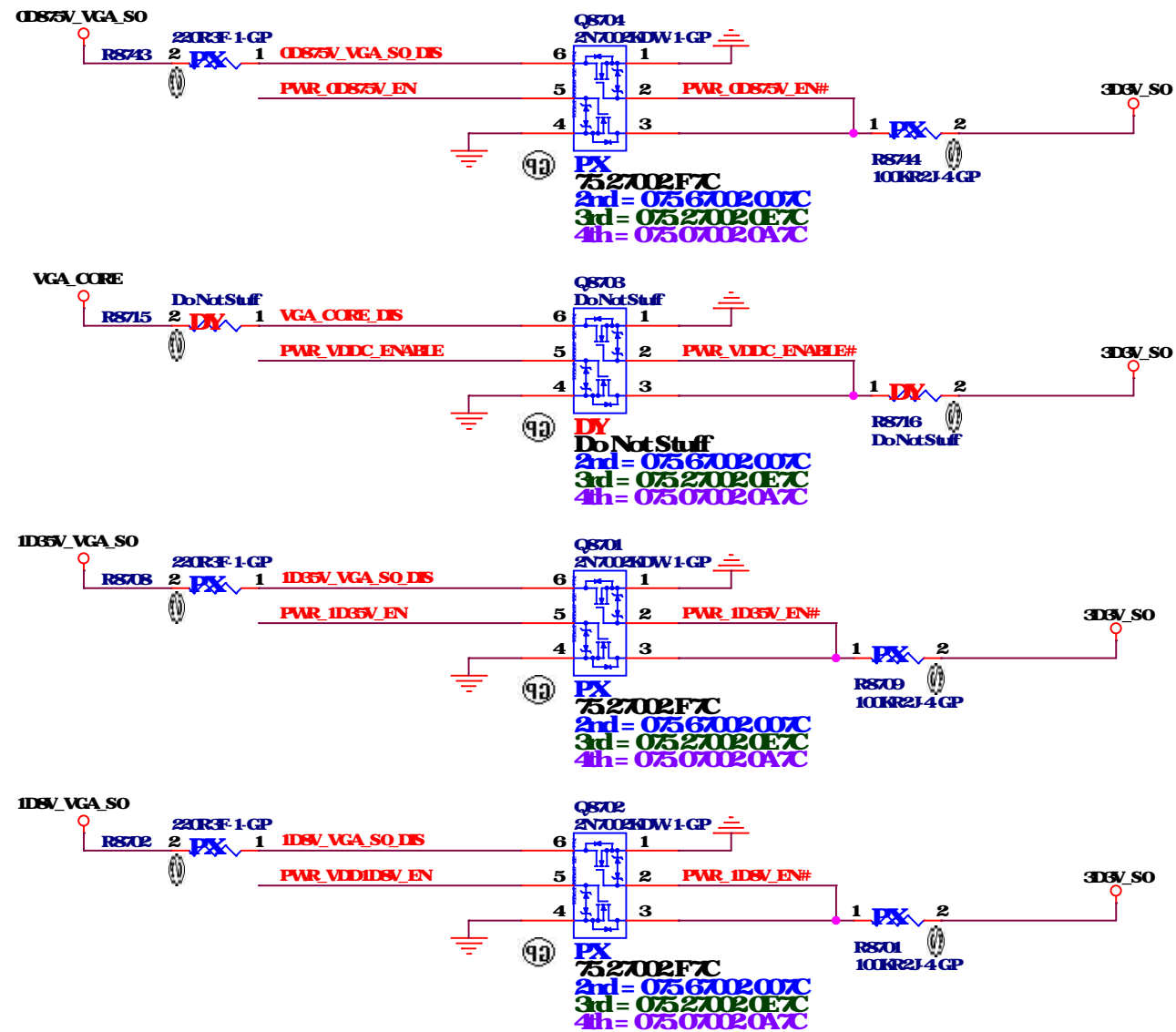
ACZ2260 For 1D35V

GPU PVR Sequencing



- All the GrU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/ μ s.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μ s before VDDC, VDDCI, VDD08, and VMEMIO start to ramp up.

86 PWR_OD875V_EN >>—
85,86 PWR_VDDC_ENABLE >>—
86 PWR_ID35V_EN >>—
86 PWR_VDDID8V_EN >>—



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GPU DISCHARGE

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Rev
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Date: Wednesday, April 17, 2009

Sheet 88 of 108



Figure 1: Schematic diagram of the proposed system architecture. The diagram illustrates the connections between the MAIN block and various components. The components are labeled as follows:

- 120L01
- 120L0100W7100
- PCIE_VMMIO
- PCIE_RSTN
- PCIE_CLKREQ_CPU_N
- PCIE_CLK_CPU_P
- PCIE_CLK_CPU_N
- PCIE_CLK_CPU_P

The connections are shown as red arrows pointing from the MAIN block to the components, with a blue circle containing a '1' indicating a specific signal or connection point.

Diagram illustrating the structure of a protein (likely a viral capsid) with 14 specific residues highlighted in blue circles and labeled on the right:

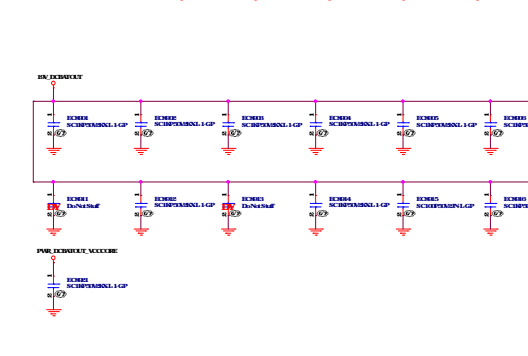
- ATPT34
- ATPT33
- ATPT40
- ATPT32
- ATPT31
- ATPT35
- ATPT36
- ATPT37
- ATPT38
- ATPT39
- ATPT46
- ATPT47
- ATPT48
- ATPT49

[illegible]

Timing diagram for the SPI interface. The diagram shows the relationship between CS (Chip Select), SCK (Serial Clock), and DATA signals. The CS signal is active-low, transitioning from high to low to initiate a transfer and back to high to end it. The SCK signal provides the clock for the data transfer. The DATA signal is sampled on the falling edge of each SCK pulse. The diagram illustrates four data transfers, with the first transfer starting at the first falling edge of SCK, indicated by a red arrow.

Figure 1

Diagram illustrating the configuration of the **IN_TTYPE_MMR** register for the **IN_TTYPE_MMR** module. The diagram shows the register value **0x00000000** and the **IN_TTYPE_MMR** register value **0x00000000**. The register is divided into four 32-bit fields, each with a value of **0x00000000**. The fields are labeled **IN_TTYPE_MMR_0**, **IN_TTYPE_MMR_1**, **IN_TTYPE_MMR_2**, and **IN_TTYPE_MMR_3**. The **IN_TTYPE_MMR_0** field is further divided into four 8-bit fields, each with a value of **0x00**. The **IN_TTYPE_MMR_1** field is further divided into four 8-bit fields, each with a value of **0x00**. The **IN_TTYPE_MMR_2** field is further divided into four 8-bit fields, each with a value of **0x00**. The **IN_TTYPE_MMR_3** field is further divided into four 8-bit fields, each with a value of **0x00**. The **IN_TTYPE_MMR** register is connected to the **IN_TTYPE_MMR** module, which is connected to the **IN_TTYPE_MMR** module.

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EXT10(RSVD)

Size
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Sheet 95 of 106

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Sheet 96 of 106

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Sheet 97 of 106

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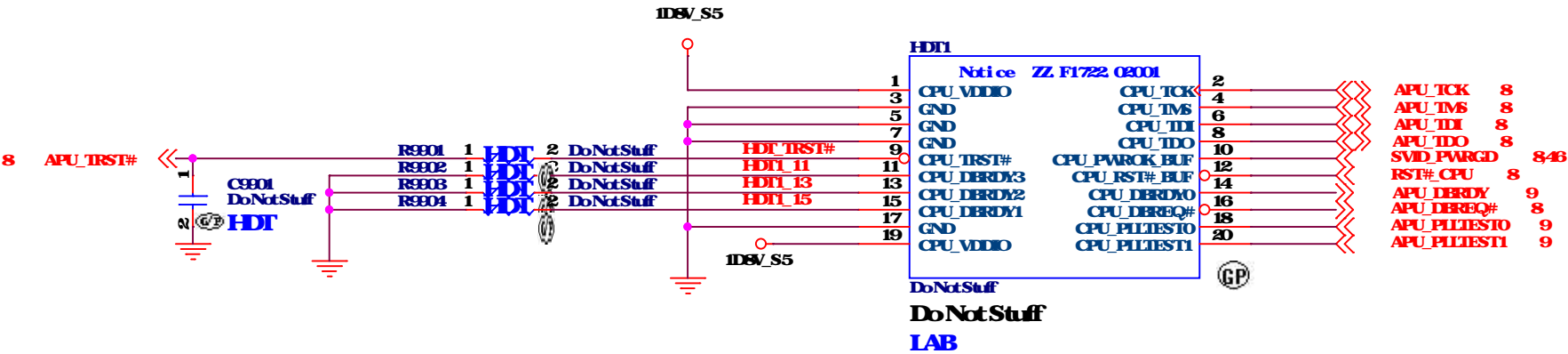
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Rev
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Date: Wednesday, April 17, 2009

Sheet 98 of 108

HDI CON



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Debug (HDI debug)			
Size	Document Number	Rev	
A4	Strongbow_PK	1	
Date	Wednesday, April 17, 2009	Sheet	99 of 106

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Table of Content

Size
A4

Document Number

Strongbow_PK

Rev
1

Date: Wednesday, April 17, 2009

Sheet 100 of 106

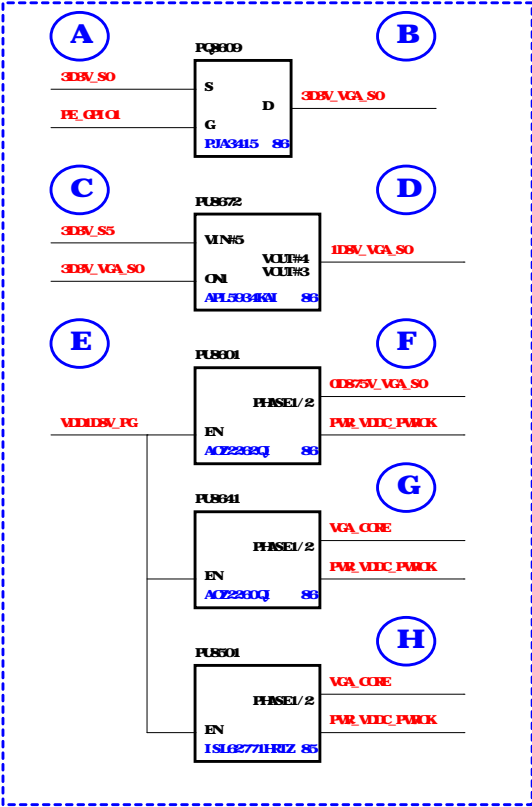
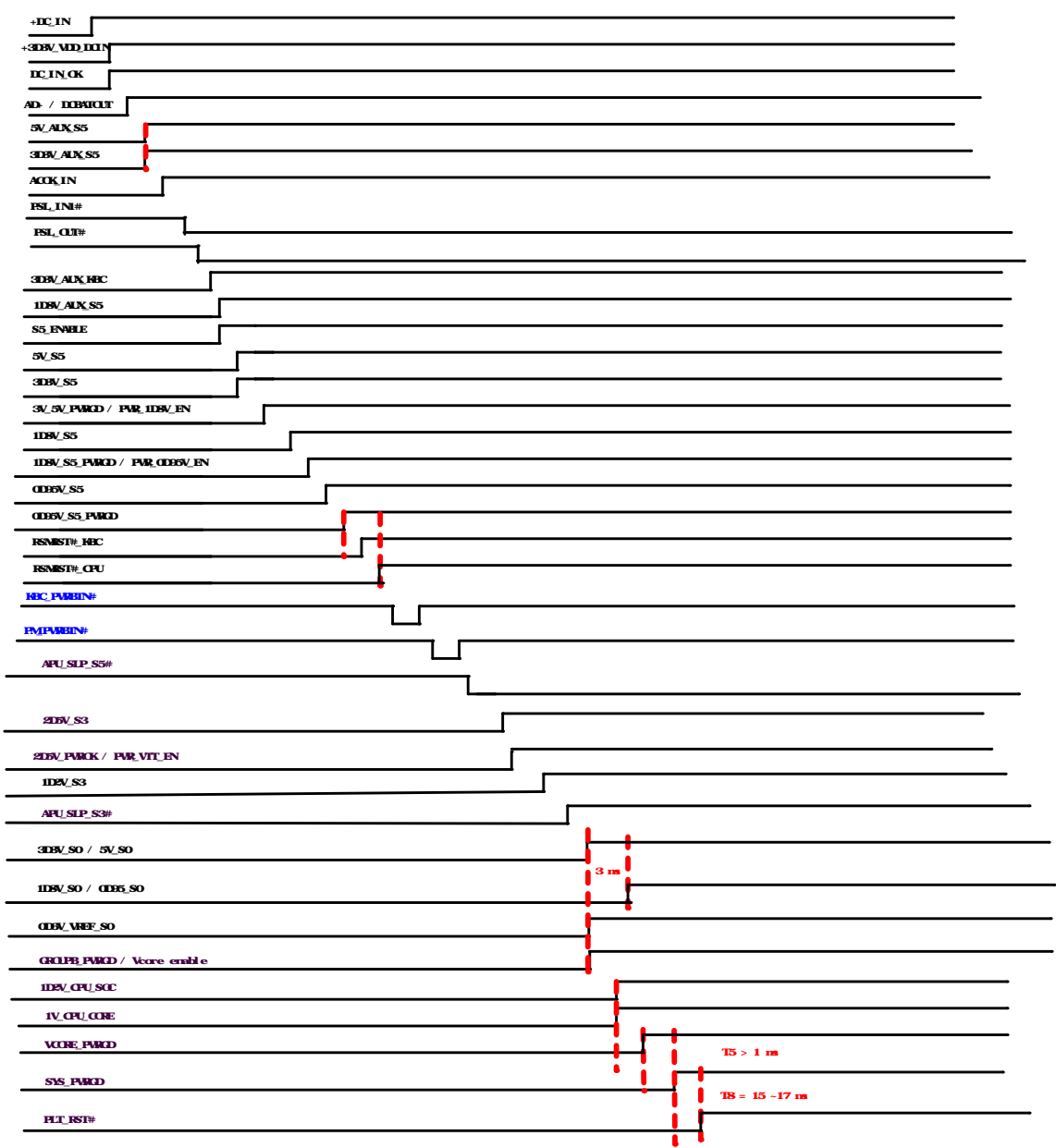
PRODUCT			CONFIGURATION									
MODEL	OPN	C TDP RANGE	CORES	THREADS	GPU CU	GPU Model	CPU CLK GHz (max/bare)	GPU Clock MHz (max)	DID	RID	Processor Type ^(a)	Display Pipe
AMD Ryzen™ 7 3700U	2M370SC4T4MFB(ES) ZM370SC4T4MFG(PC) YM3700C4T4MFG(PR)	12-35w	4	8	10	AMD Radeon™ RX Vega 10 Graphics	4.0/2.3 ^(b)	1400 ^(b)	15D8	C1	Type1	4
AMD Ryzen™ 5 3500U	ZM350SC4T4MFG(PC) YM3500C4T4MFG(PR)	12-35w	4	8	8	AMD Radeon™ Vega 8 Graphics	3.7/2.1 ^(b)	1200 ^(b)	15D8	C2	Type1	4
AMD Ryzen™ 3 3300U	ZM330SC4T4MFG(PC) YM3300C4T4MFG(PR)	12-35w	4	4	6	AMD Radeon™ Vega 6 Graphics	3.5/2.1 ^(b)	1200 ^(b)	15D8	C3	Type1	4
AMD Ryzen™ 3 3200U	ZM320SC4T2OFG(PC) YM3200C4T2OFG(PR)	12-25w	2	4	3	AMD Radeon™ Vega 3 Graphics	3.5/2.6 ^(b)	1200 ^(b)	15D8	C4	Type2	3
AMD Athlon™ 300U ^(c)	ZM300SC4T2OFG(PC) YM300UC4T2OFG(PR)	12-25W	2	4	3	AMD Radeon™ Vega 3 Graphics	3.3/2.4 ^(b)	1000 ^(b)	15D8	C5	Type2	3

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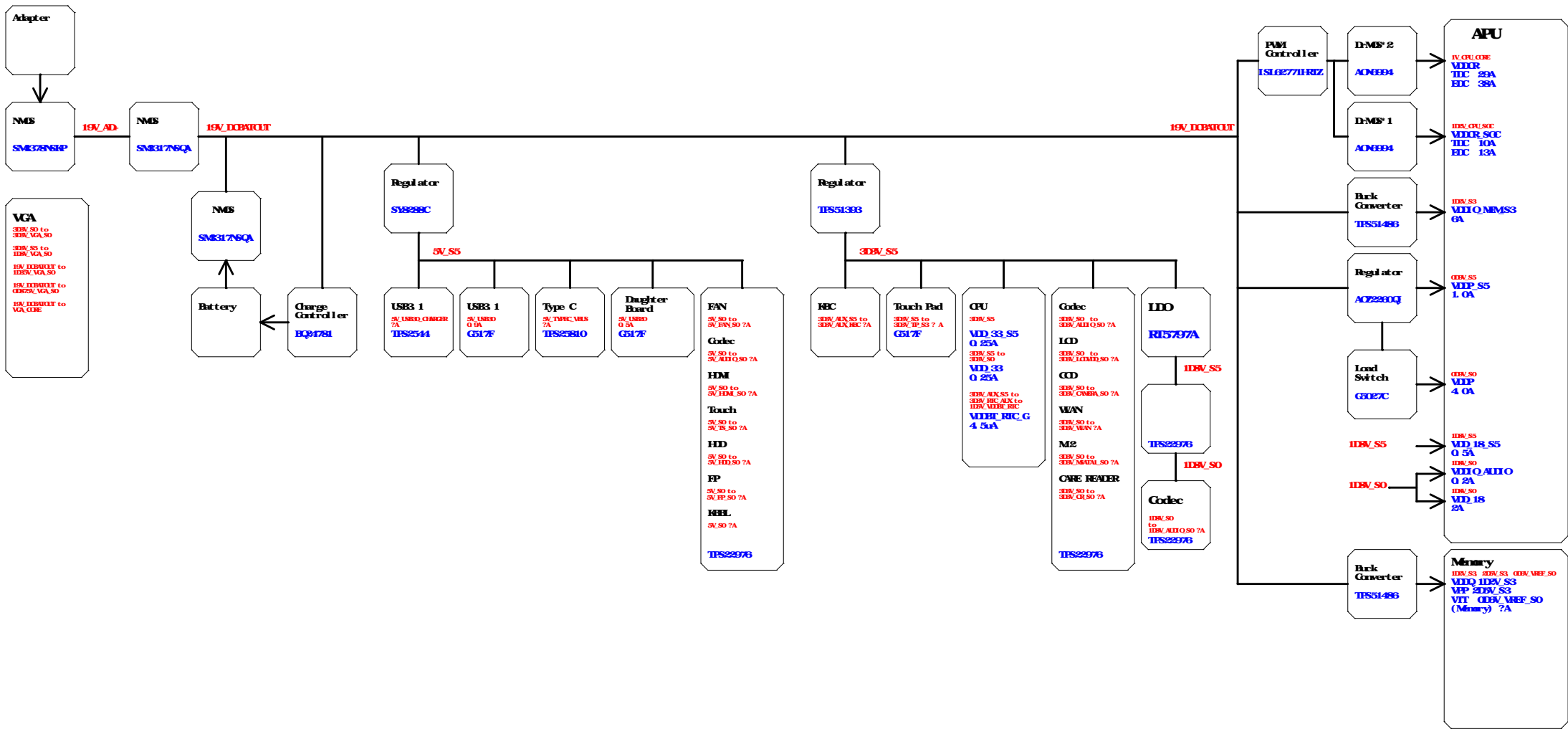
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Title			
Change History			
Size A4	Document Number Strongbow_PK		Rev 1
Date	Wednesday, April 17, 2019	Sheet 101 of	106

AC mode

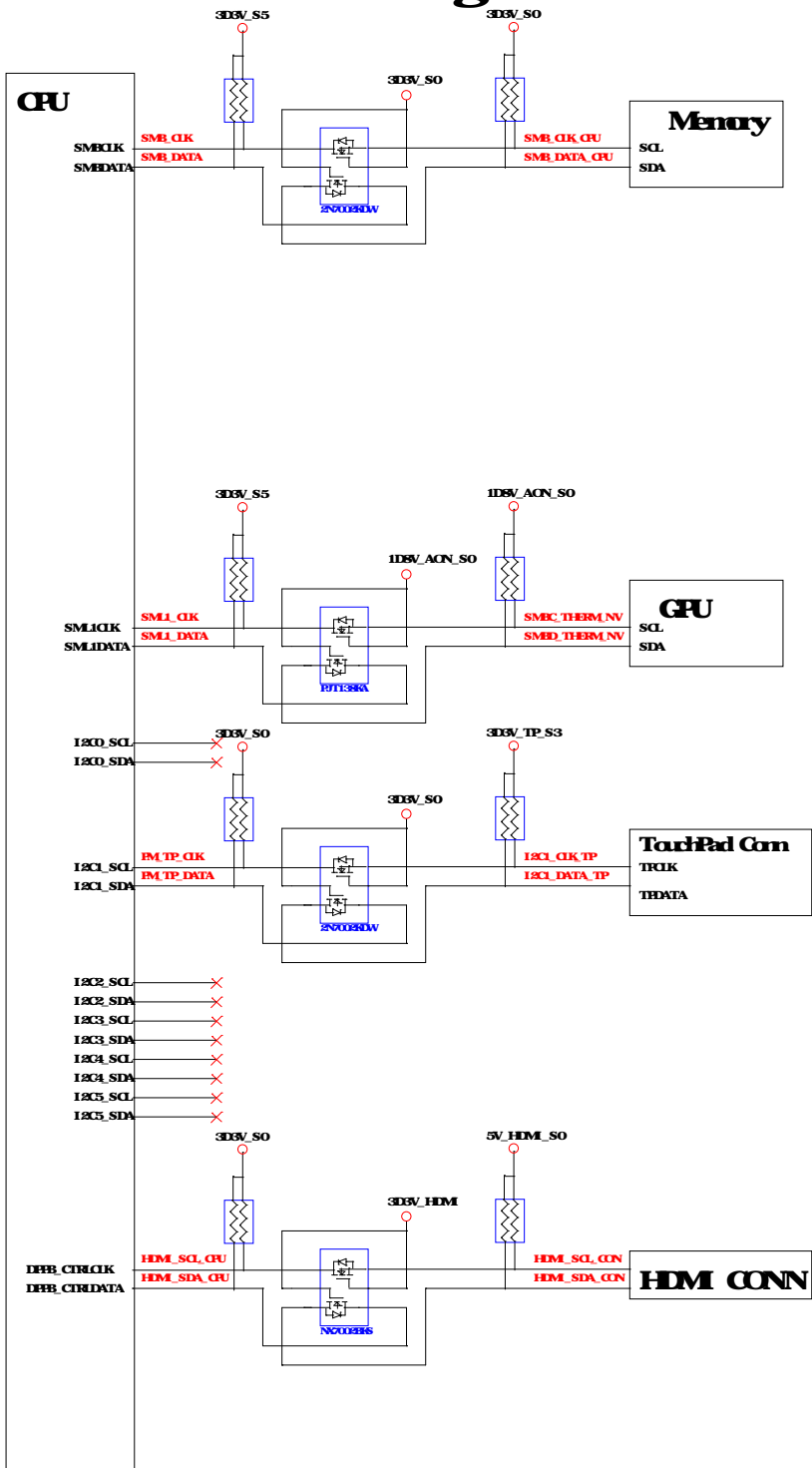


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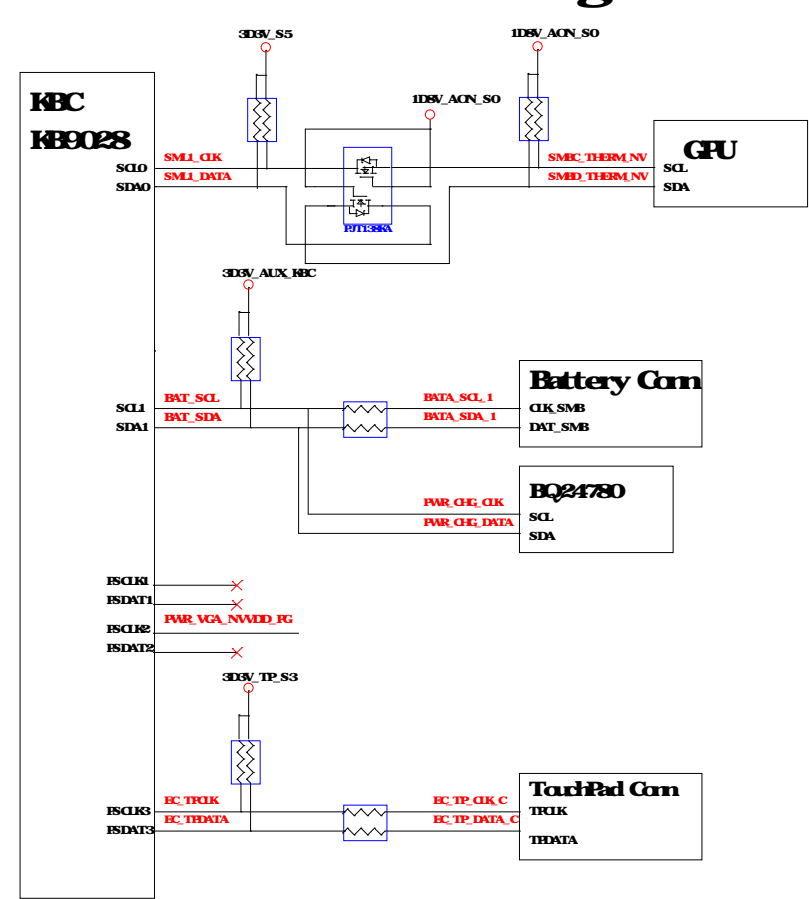
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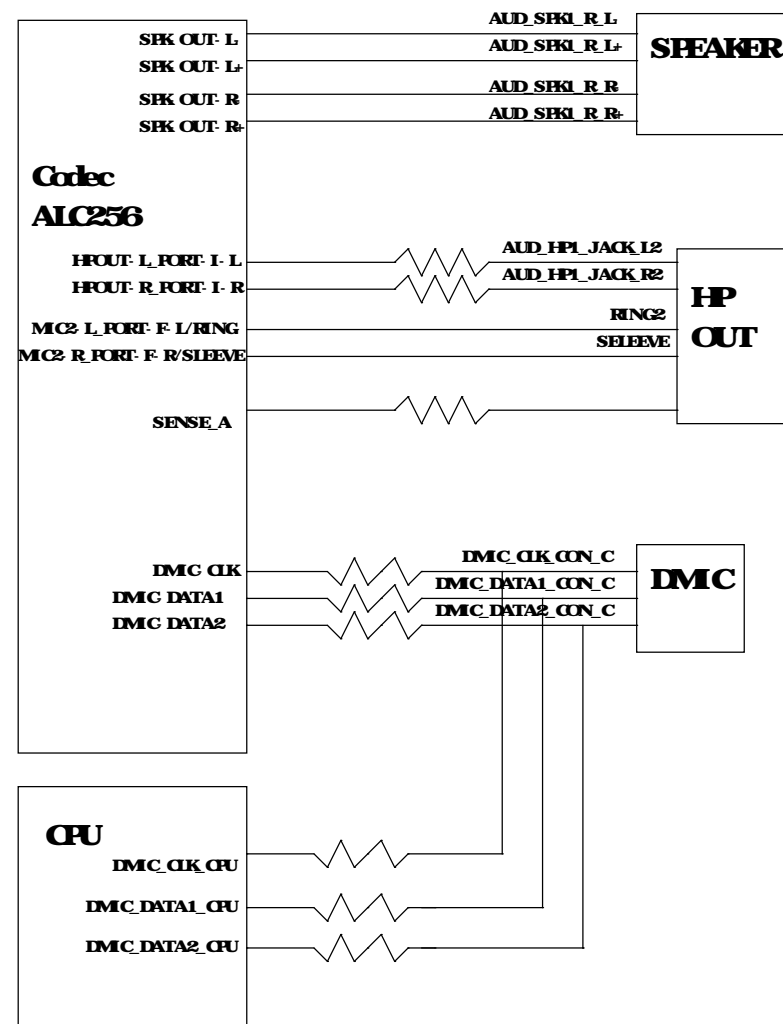
SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



Audio Block Diagram



CLOCK BLOCK DIAGRAM

